

# Foxconn Precision Co. Inc.

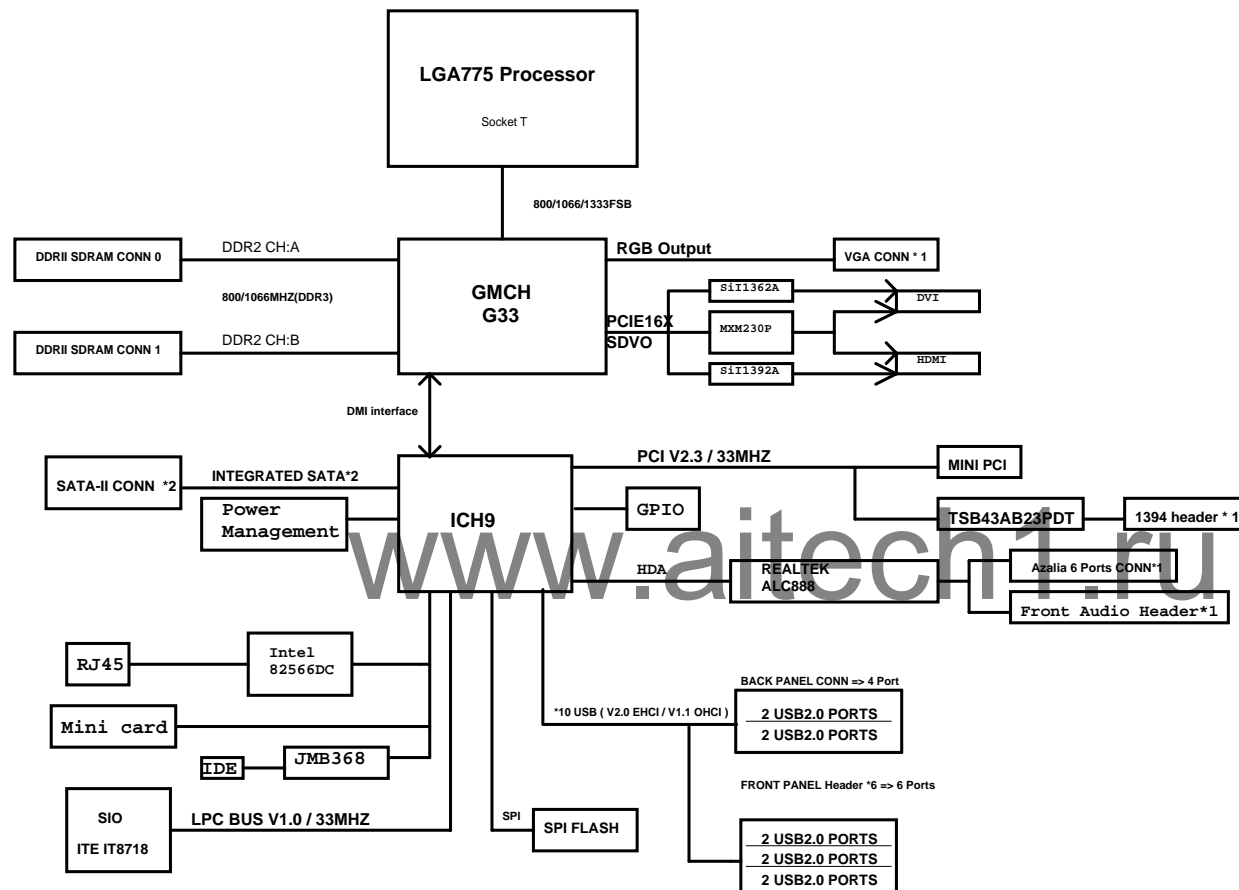
## G33S01 FAB B1 Schematic

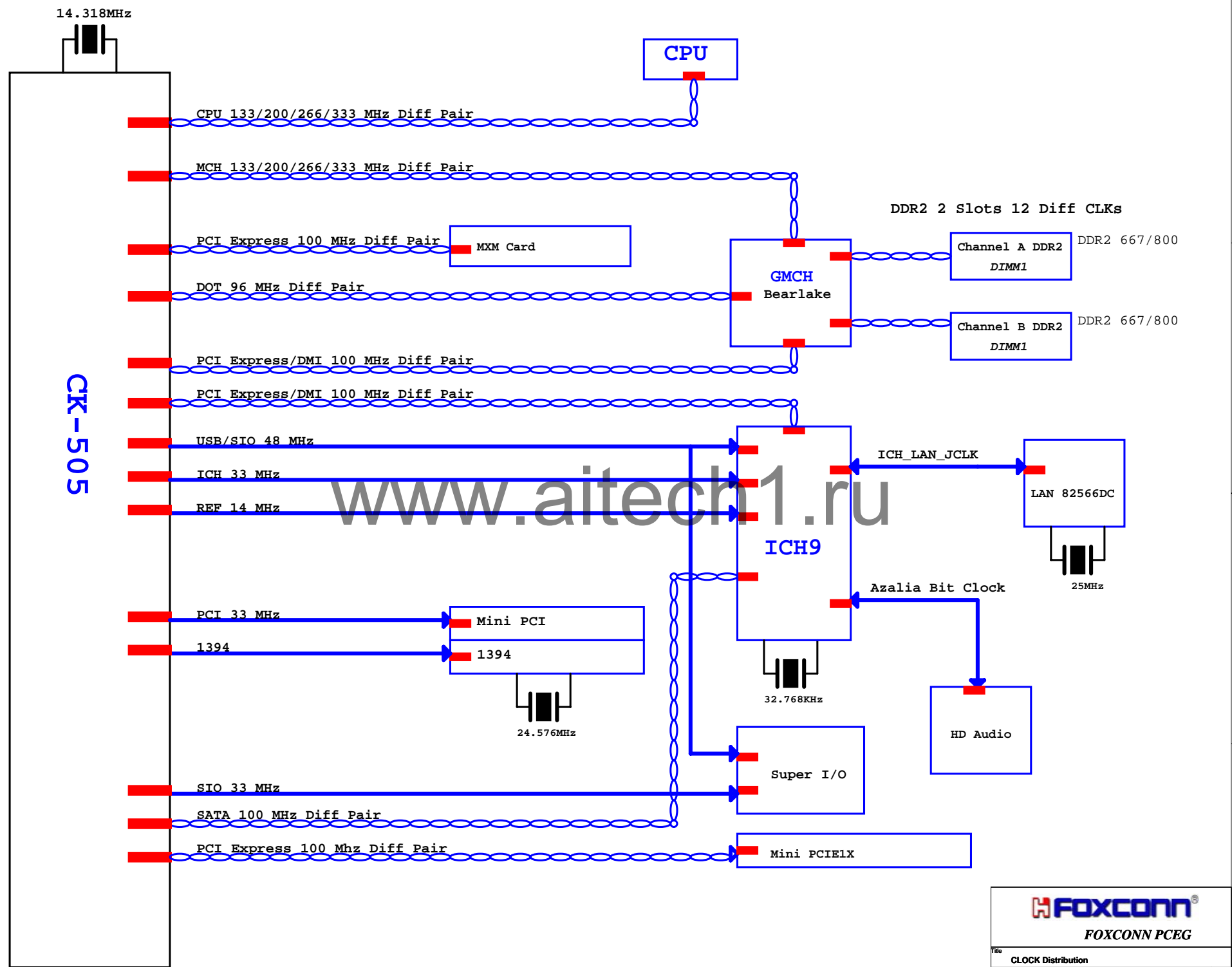
### Page Index

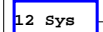
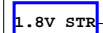
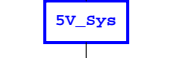
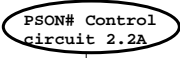
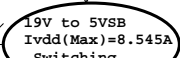
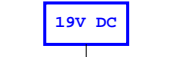
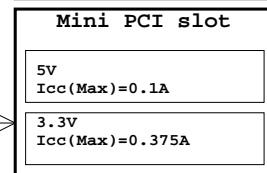
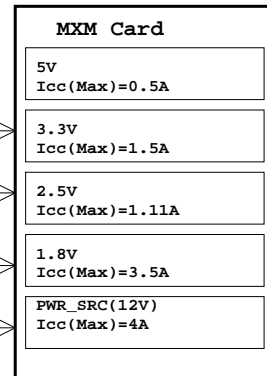
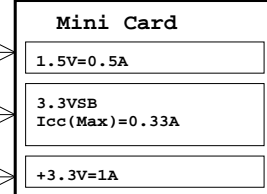
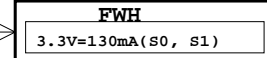
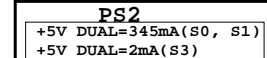
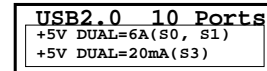
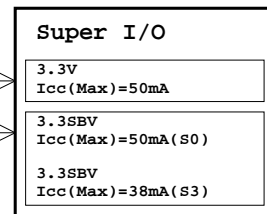
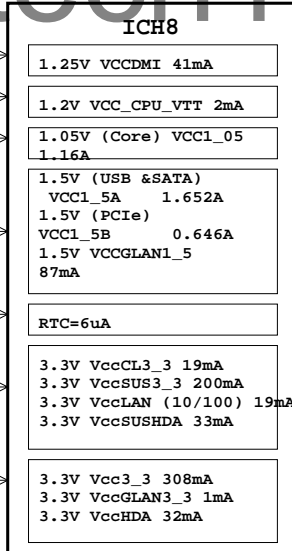
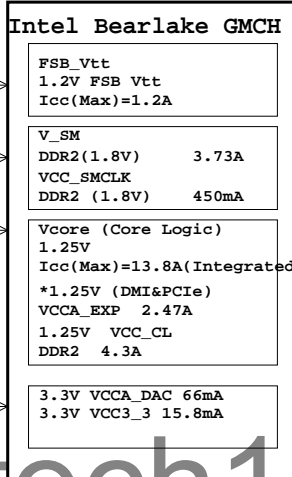
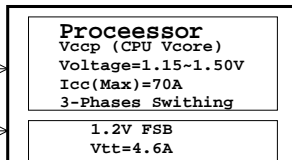
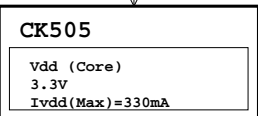
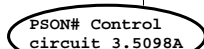
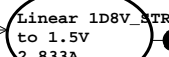
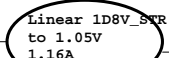
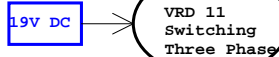
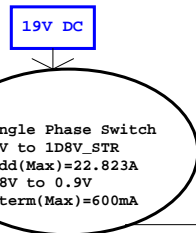
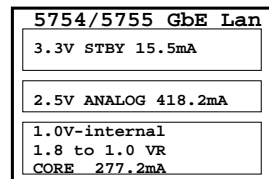
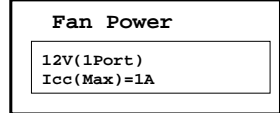
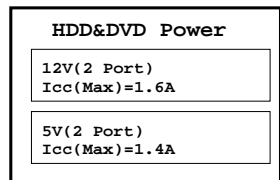
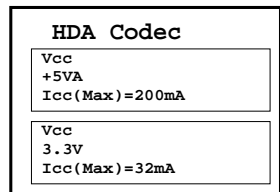
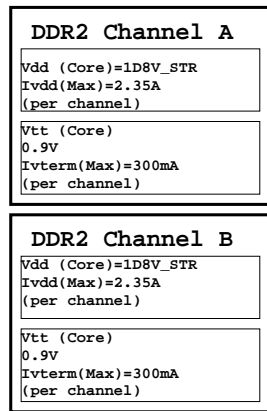
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SKU	Configuration	Board ID
G33S01	w/o MXM, w/i D-Sub	GPIO33 : Low , GPIO34 : Low
G33S01	w/o MXM, w/i DVI-I, w/i HDMI	GPIO33 : High , GPIO34 :Low
G33S01	w/i MXM, w/i DVI-I, w/i HDMI	GPIO33 : Low , GPIO34 : High

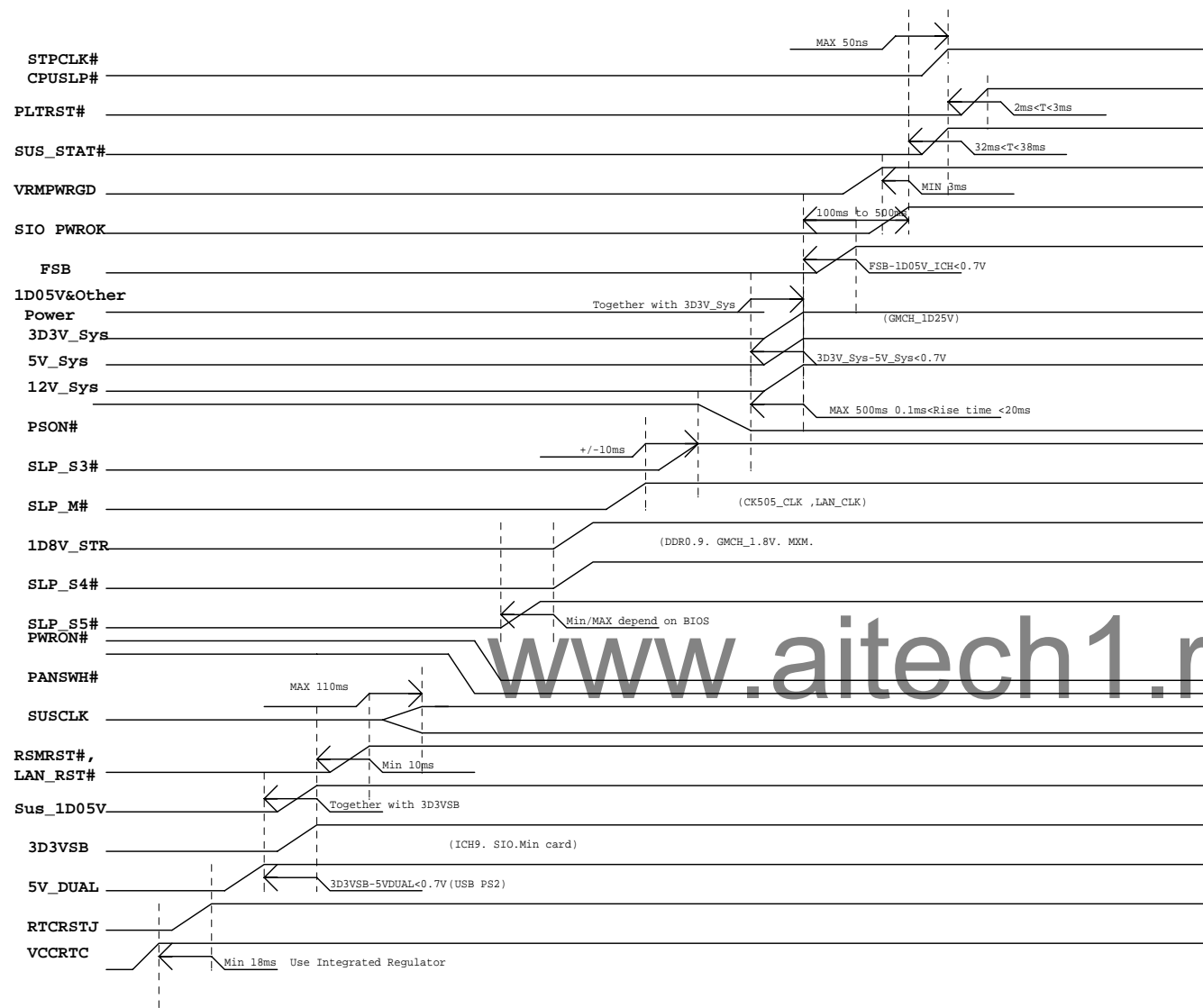
# Block Diagram





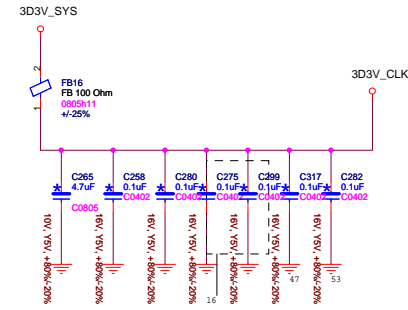
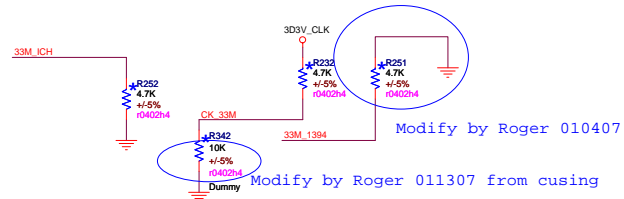
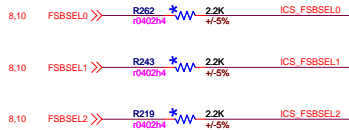


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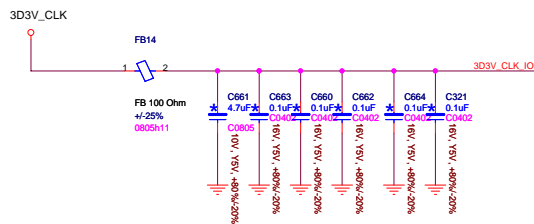
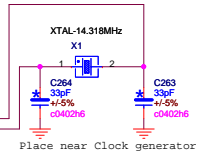
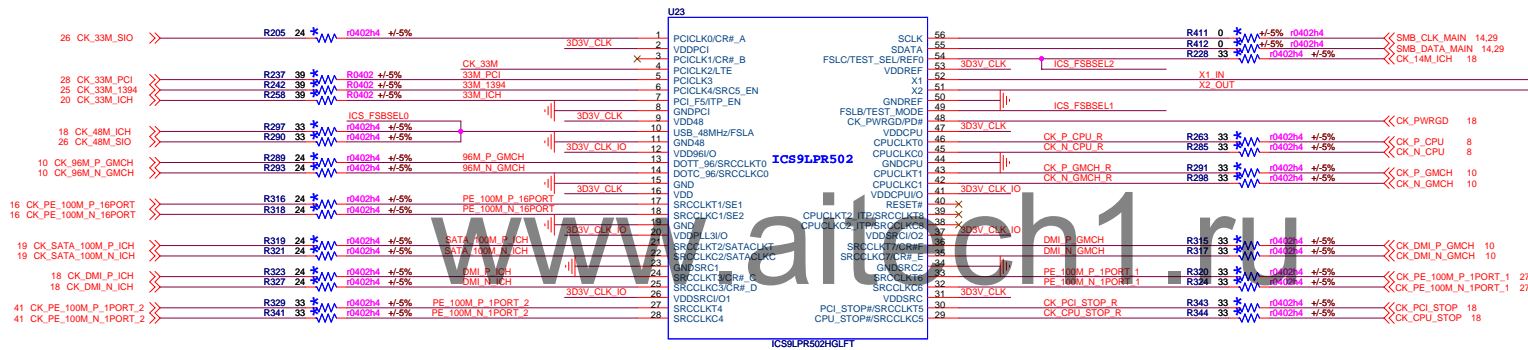


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Title			
Power sequence			
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$$C_{in} = 2 * CL - C_{in} - C_{in} = 2 * 20pf - 2.8pf - 5pf = 32.2pf$$



FSB\_VTT

R263

470

FSBSEL0

FSBSEL0

8,10

R248

470

FSBSEL1

FSBSEL1

8,10

R282

470

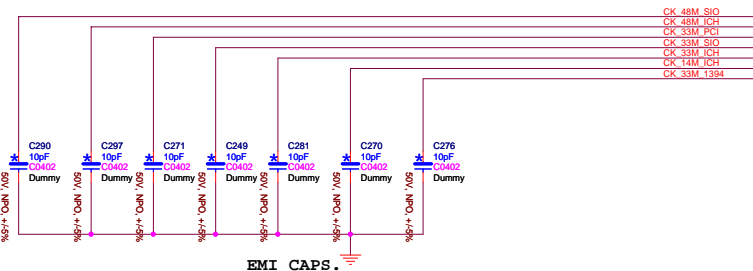
FSBSEL2

FSBSEL2

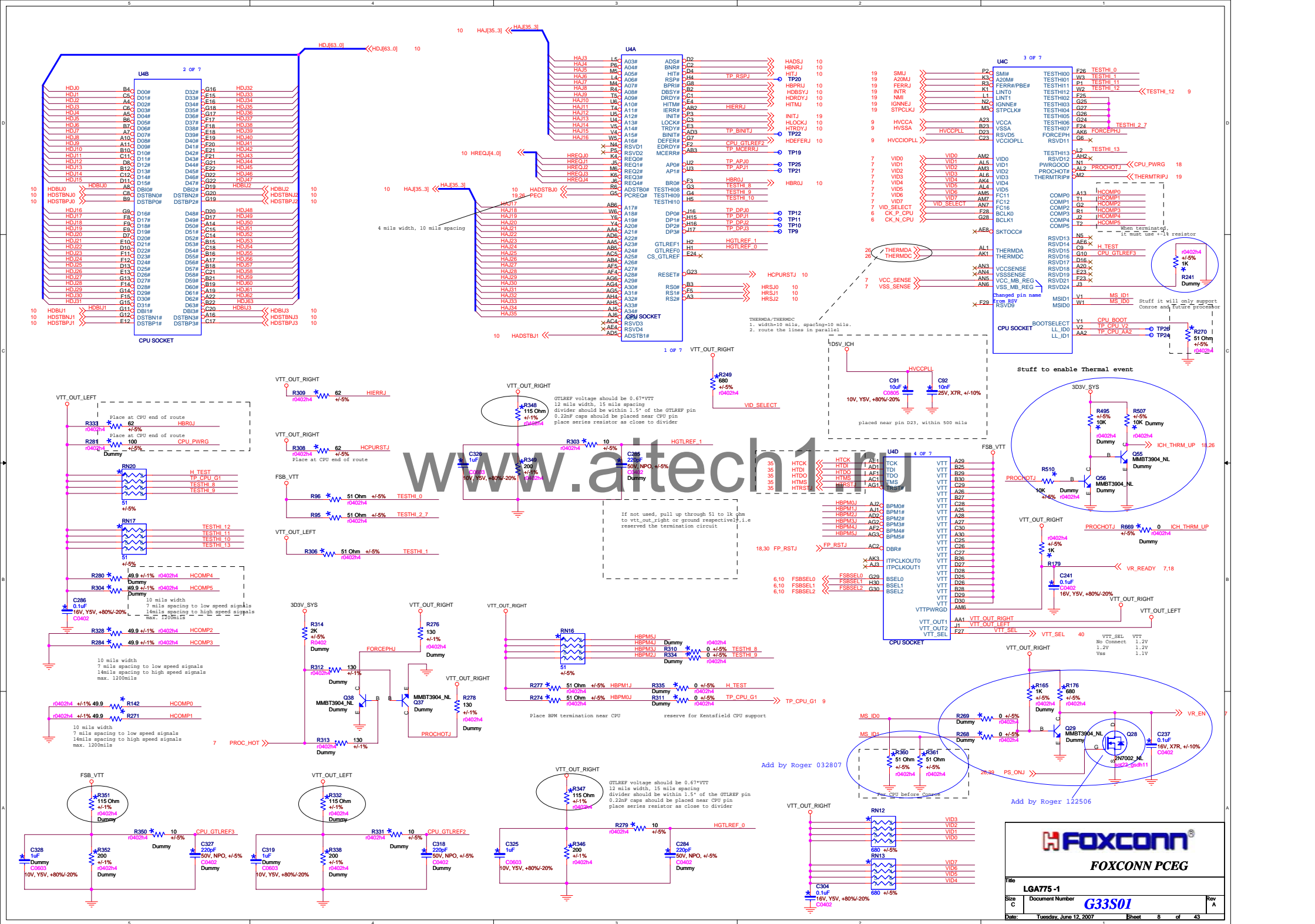
8,10

BSEL TABLE

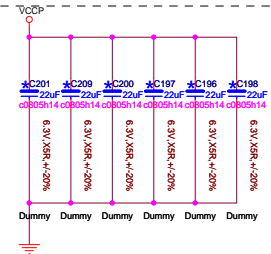
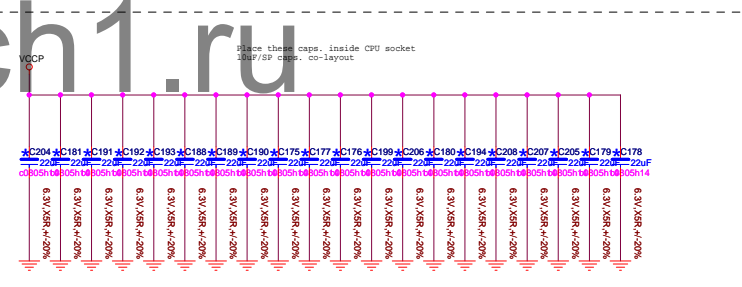
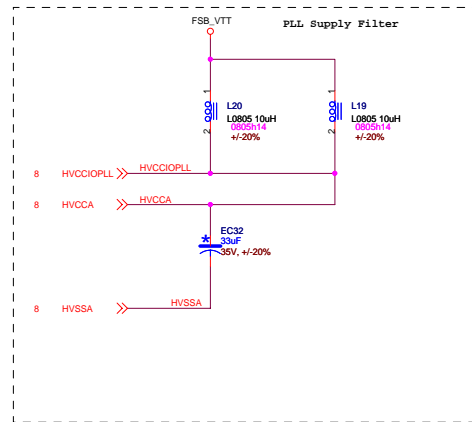
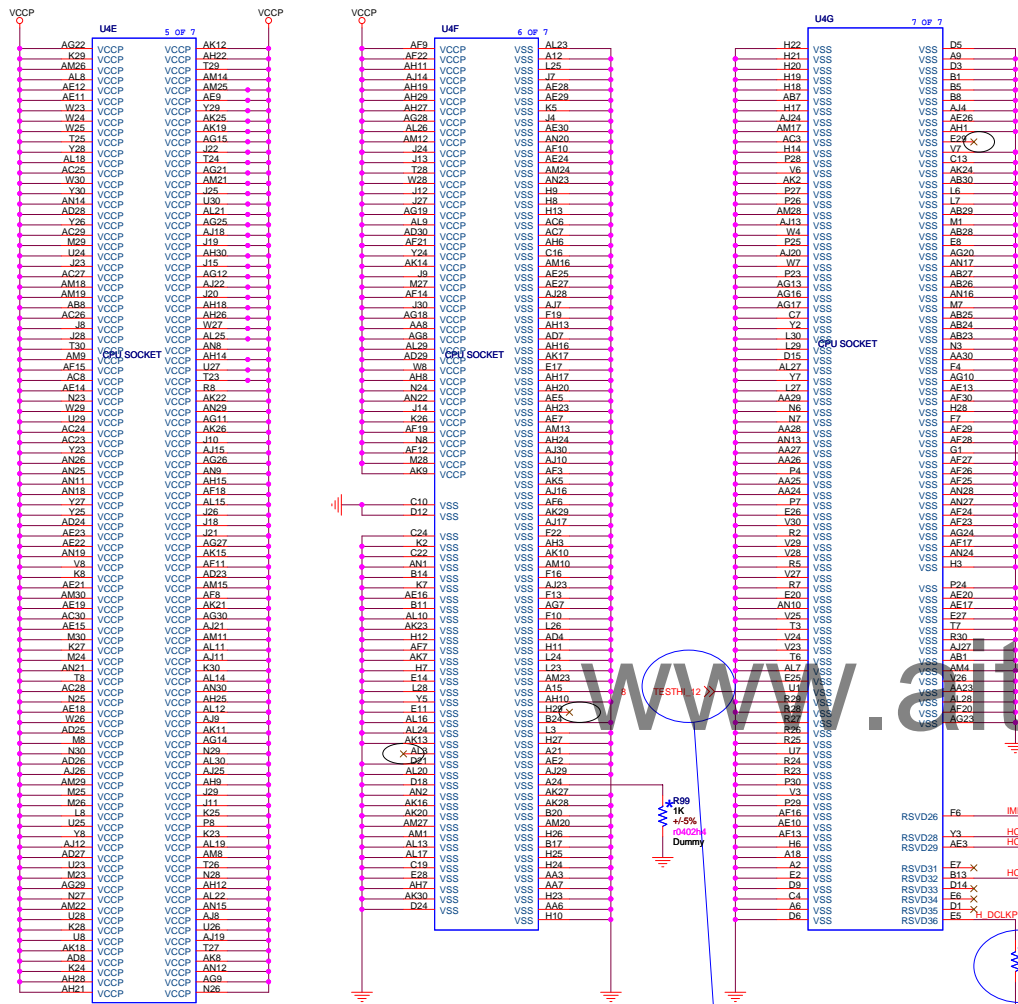
FS_CFS_BFS_A	FSB Frequency
0 1 0	200MHz (800)
0 0 0	266MHz (1066)
1 0 0	333MHz (1333)



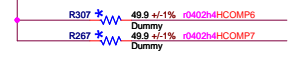








VTT\_OUT\_RIGHT

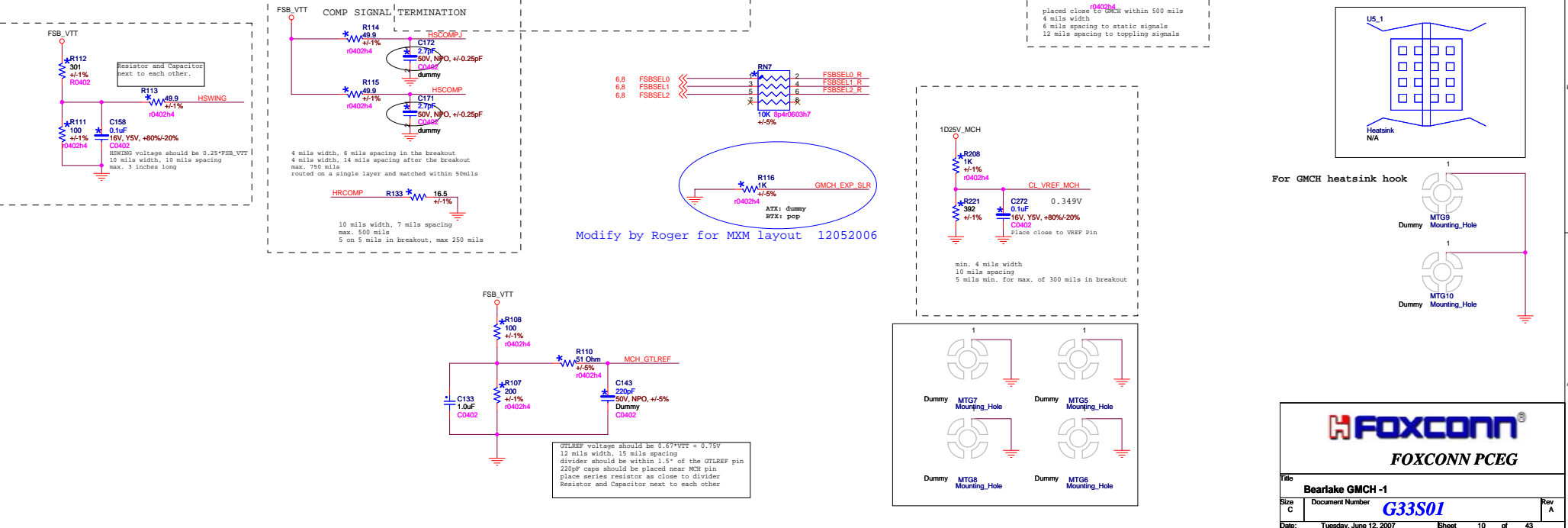


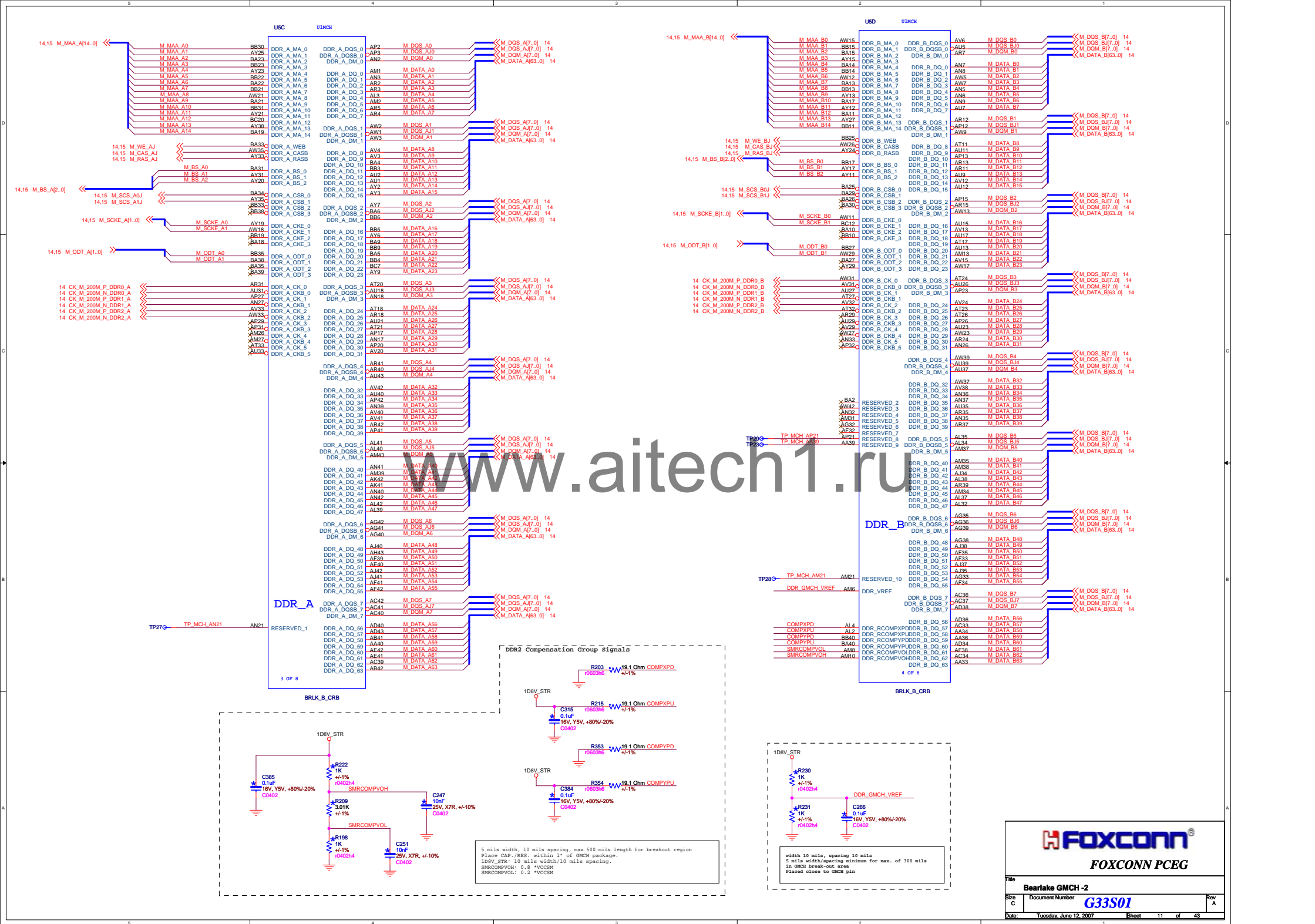
10 mils width  
7 mils spacing to low speed signals  
14mils spacing to high speed signals  
max. 1200mils

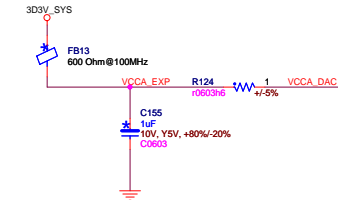
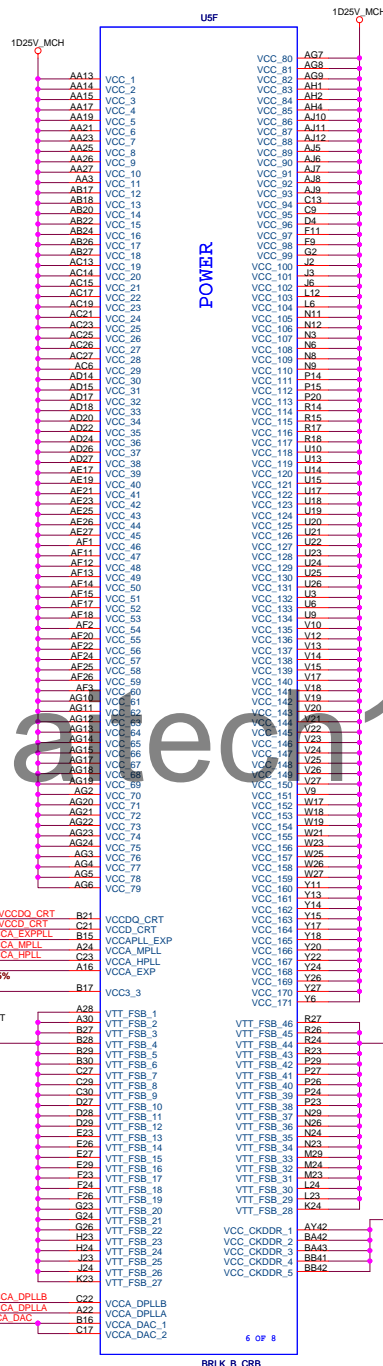
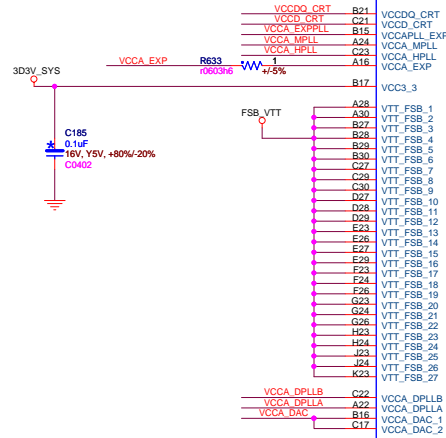
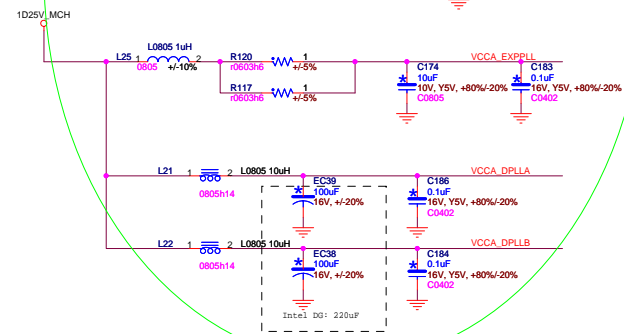
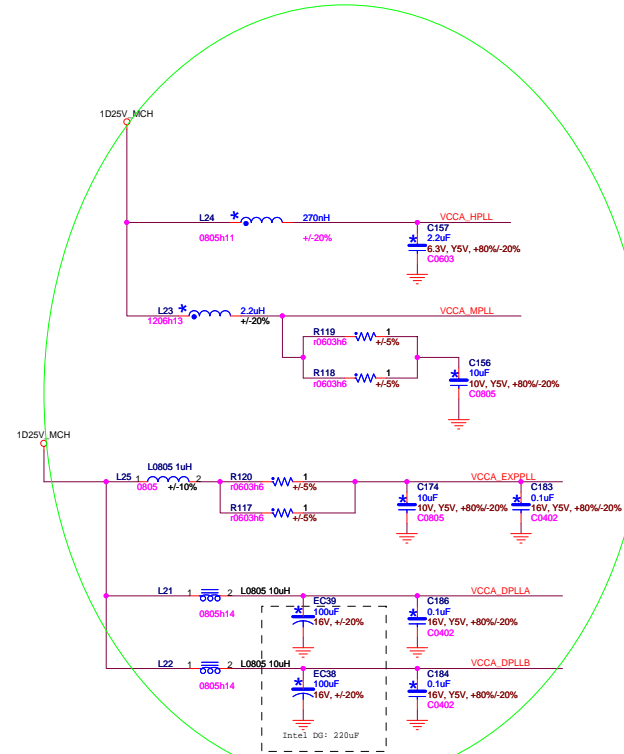
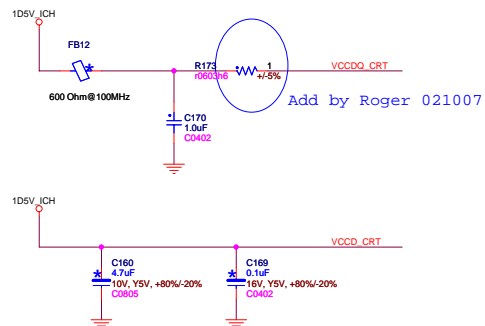
15 mils width  
7 mils spacing to low speed signals  
14mils spacing to high speed signals  
max. 1200mils

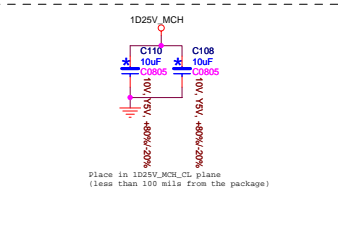
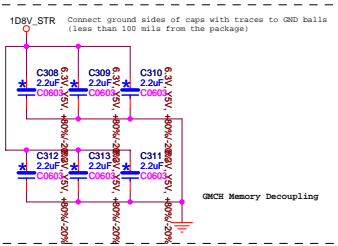
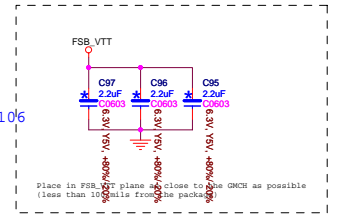
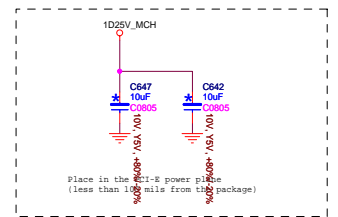
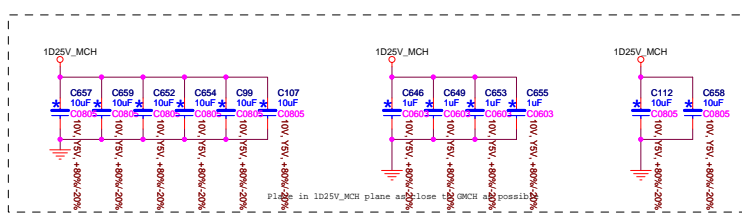
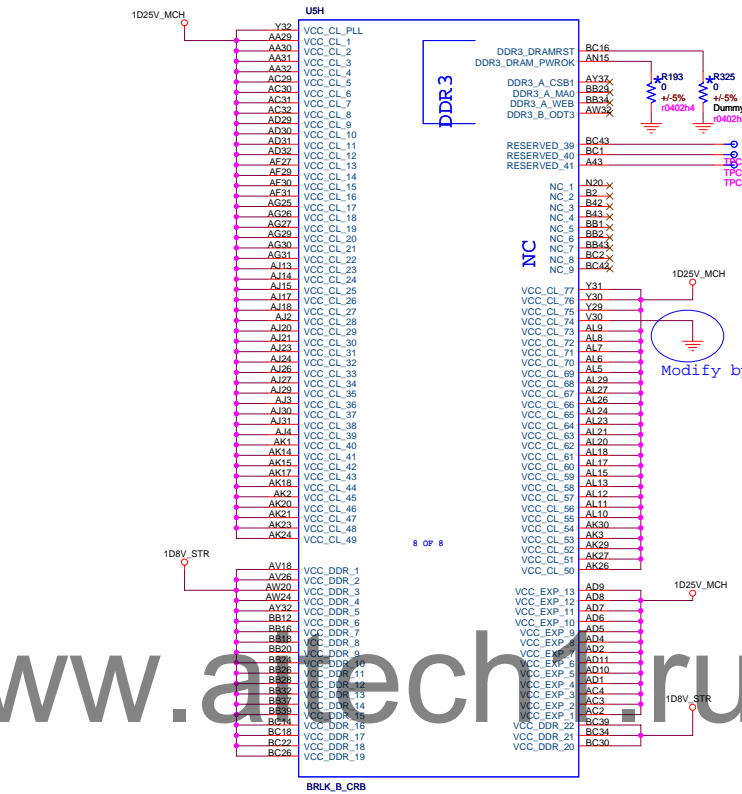
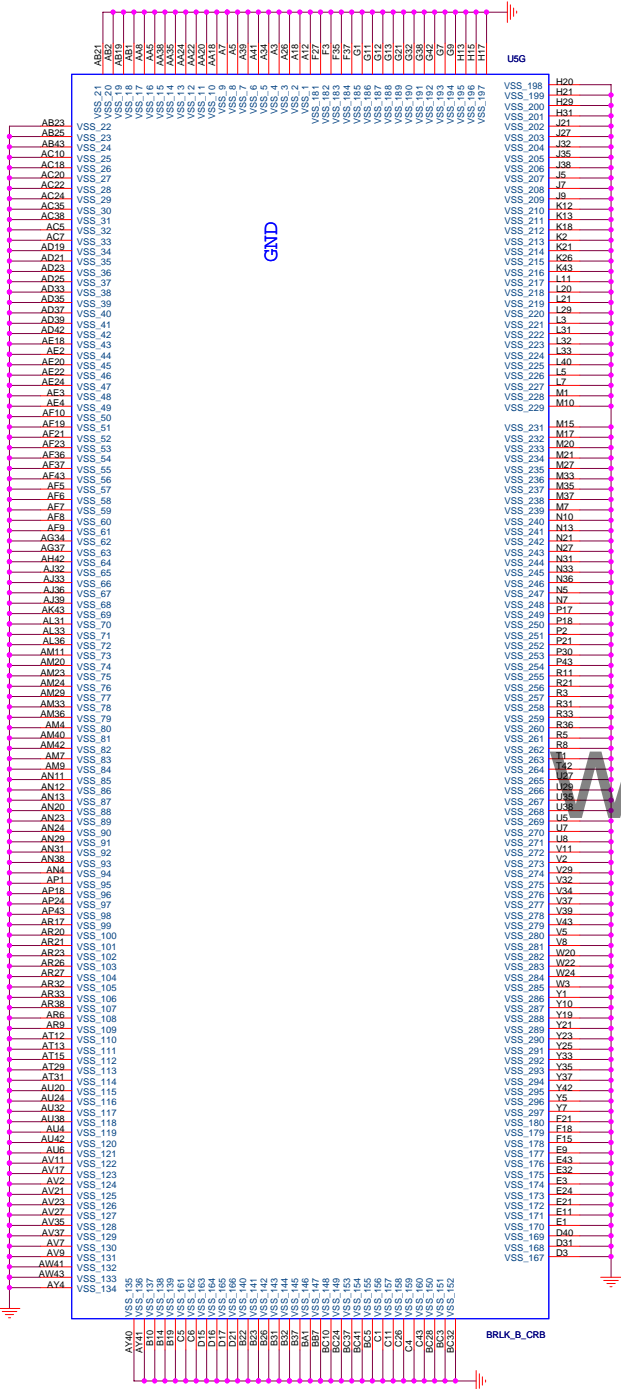


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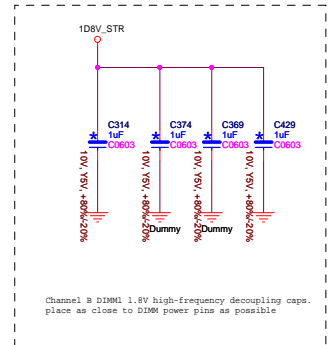
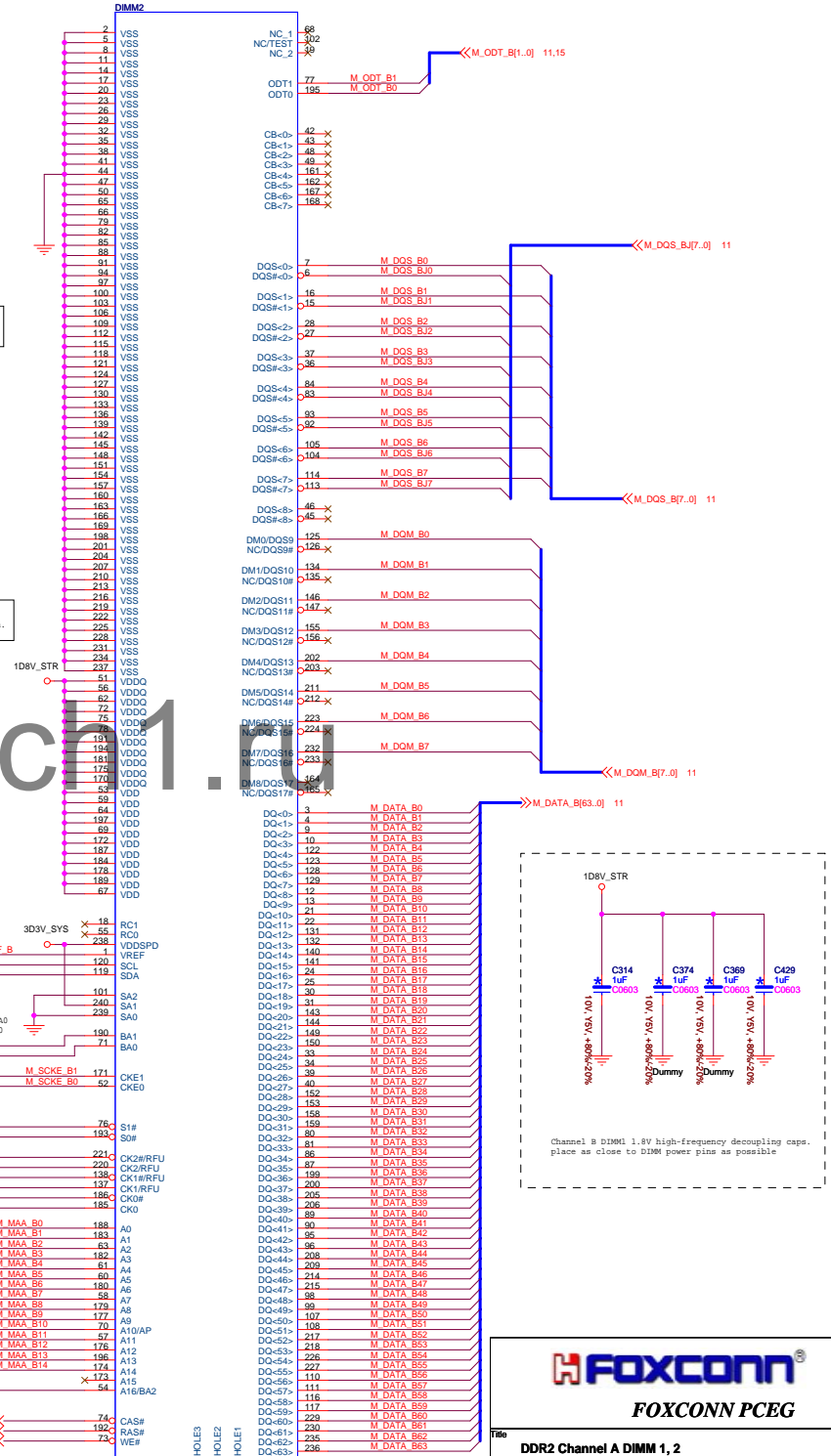
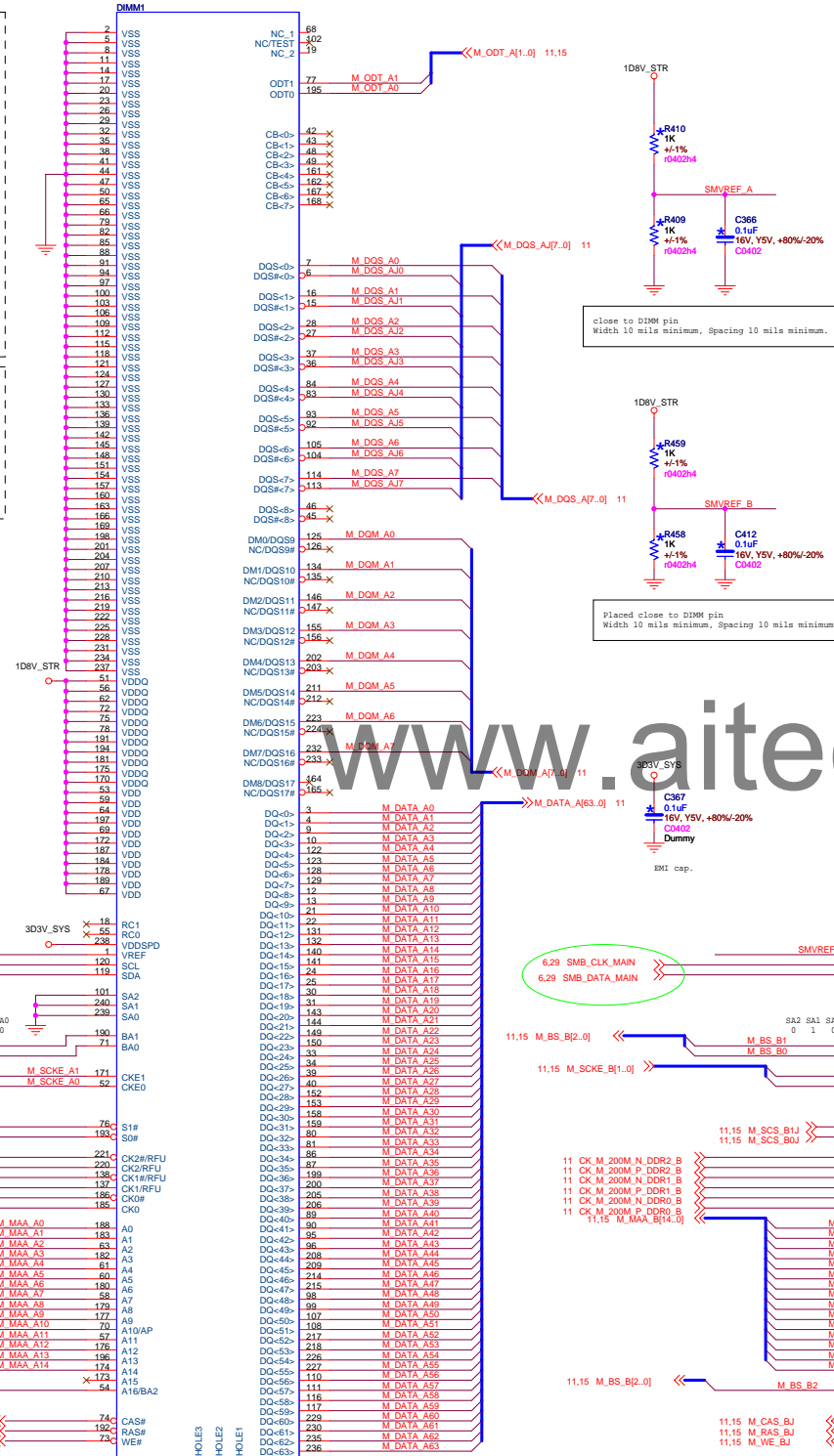
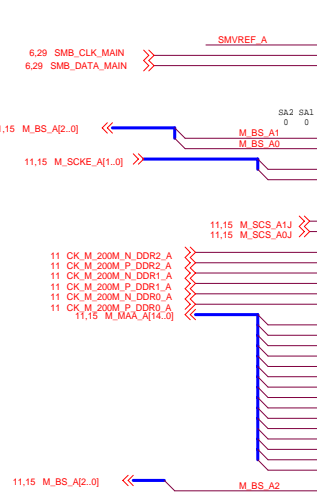
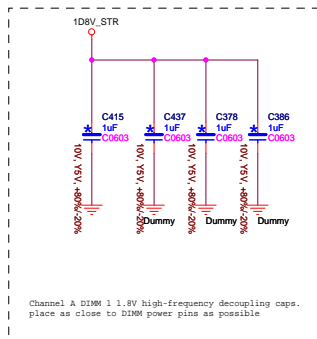


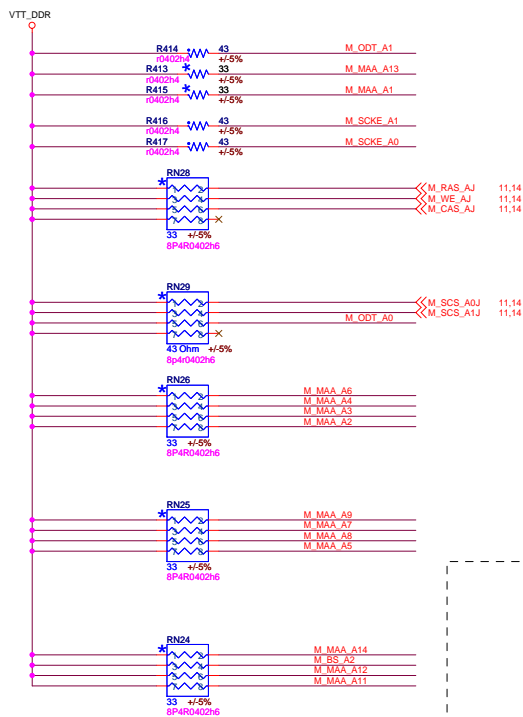




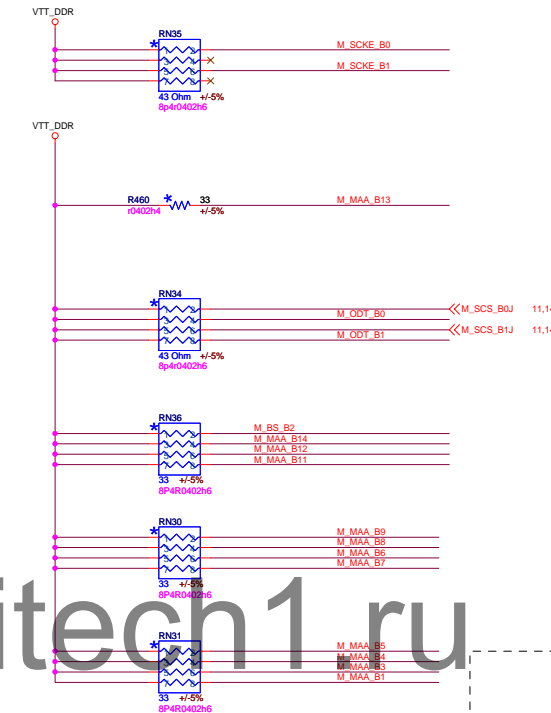
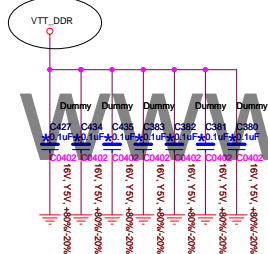
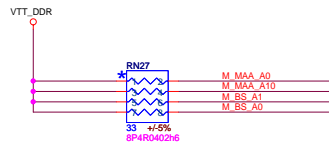




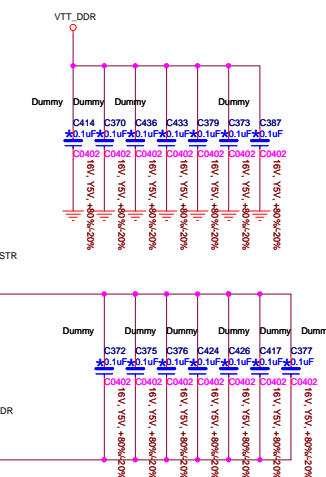
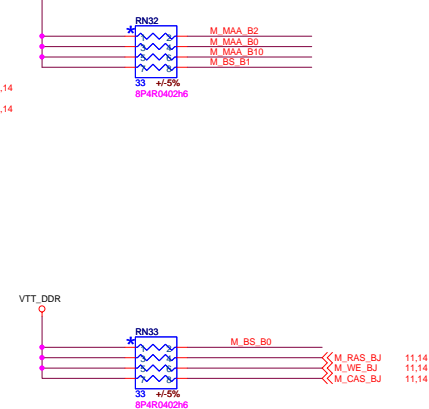




<< M\_ODT\_A[1..0] 11,14  
 << M\_SCKE\_A[1..0] 11,14  
 << M\_BS\_A[2..0] 11,14  
 << M\_MAA\_A[14..0] 11,14



<< M\_SCKE\_B[1..0] 11,14  
 << M\_BS\_B[2..0] 11,14  
 << M\_MAA\_B[14..0] 11,14  
 << M\_ODT\_B[1..0] 11,14



Channel A VTT\_0.9V Mid Range decoupling caps. Placed in termination Island

Channel A VTT\_0.9V high-frequency decoupling caps. Place as close to termination resistors as possible

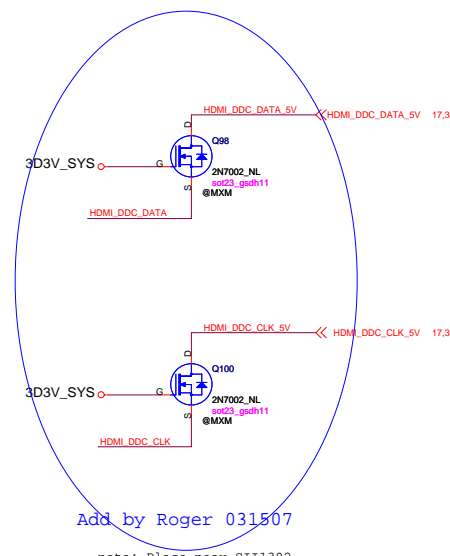
Channel B VTT\_0.9V Mid Range decoupling caps. Placed in termination Island

Channel B VTT\_0.9V high-frequency decoupling caps. Place as close to termination resistors as possible

**FOXCONN**

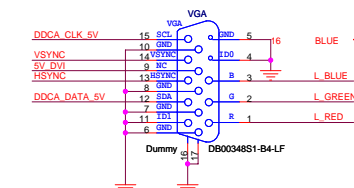
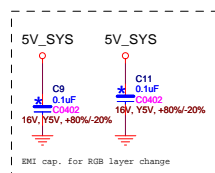
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Title		
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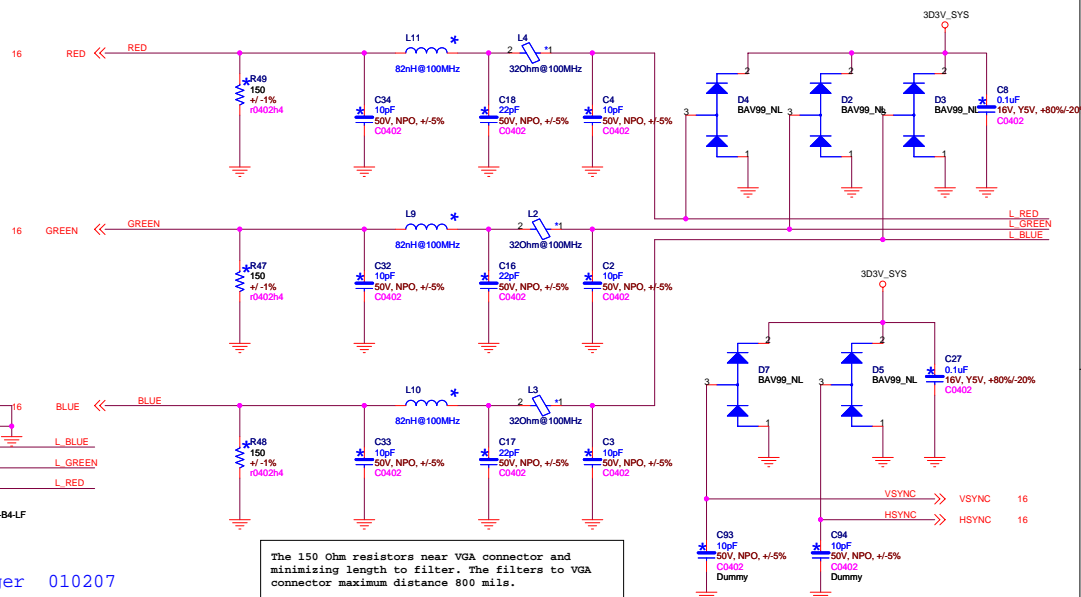




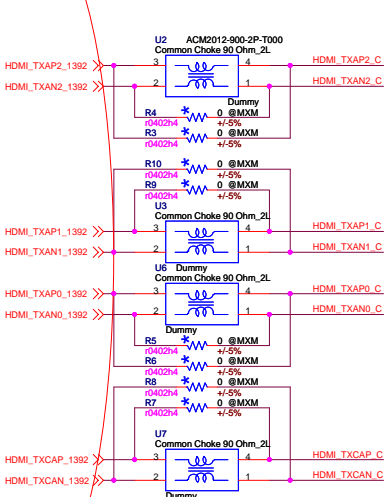
1. from GMCHC to the first 150 ohm resistor: 7.5 mils(min. 6 mils spacing )
2. from the first 150 ohm res. to the second 150 ohm resistor: 4 mils
3. from the second 150 ohm resistor to connector: 4 mils
4. spacing minimum 6 mils, 30 mils spacing is recommended
5. R<sub>G</sub>,B should be length matched to 700 mils, max. length is 8400 mils
6. R<sub>G</sub>,B signals should be ground referenced



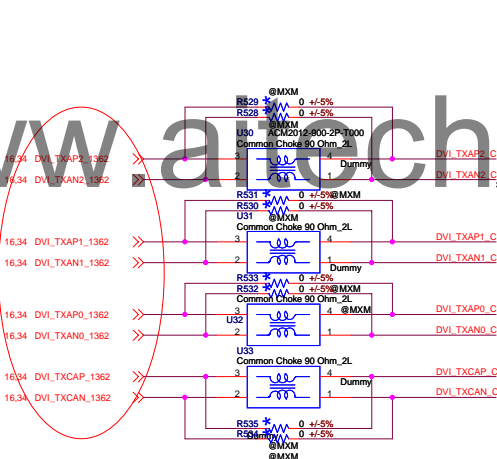
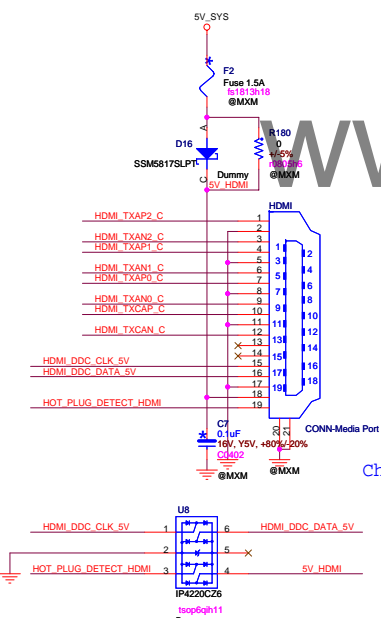
Delete DVI DDC by Roger 010207



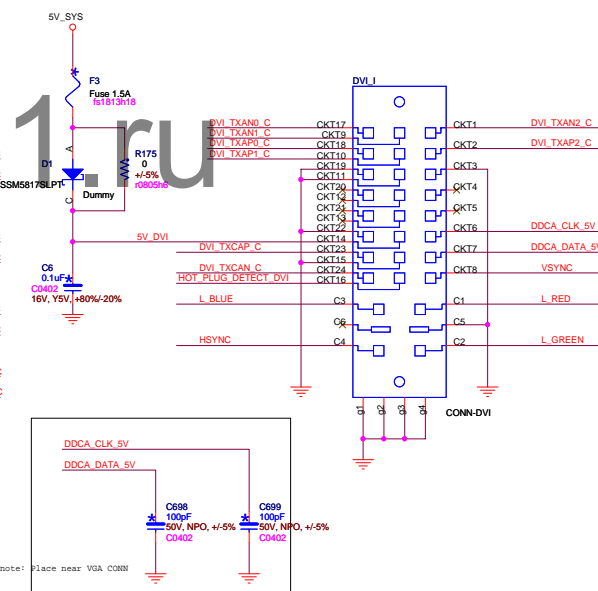
The 150 Ohm resistors near VGA connector minimizing length to filter. The filter connector maximum distance 800 mils.



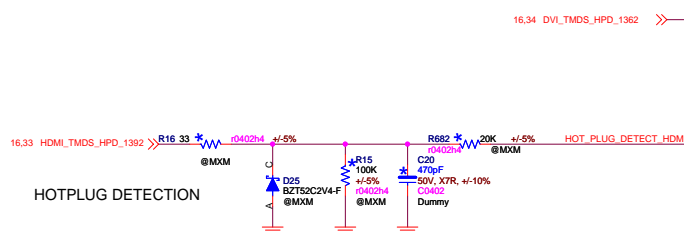
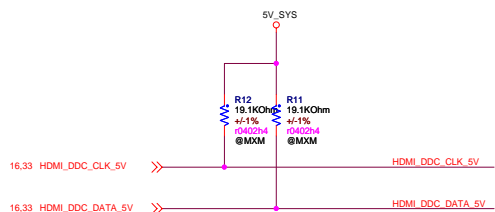
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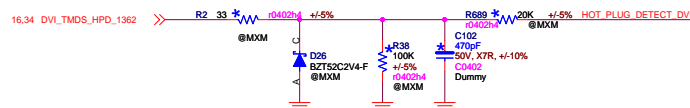
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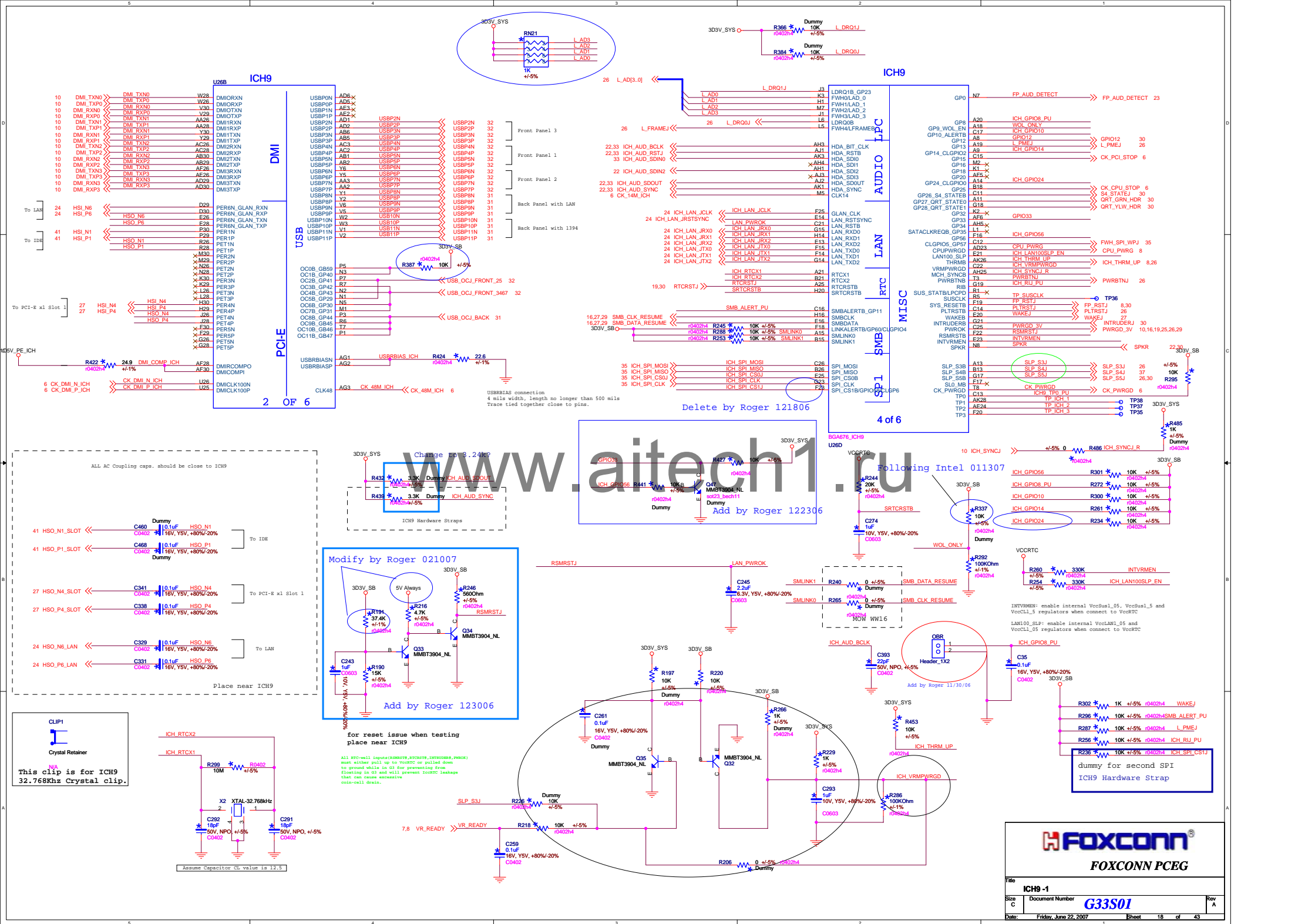
note: Place near VGA CO



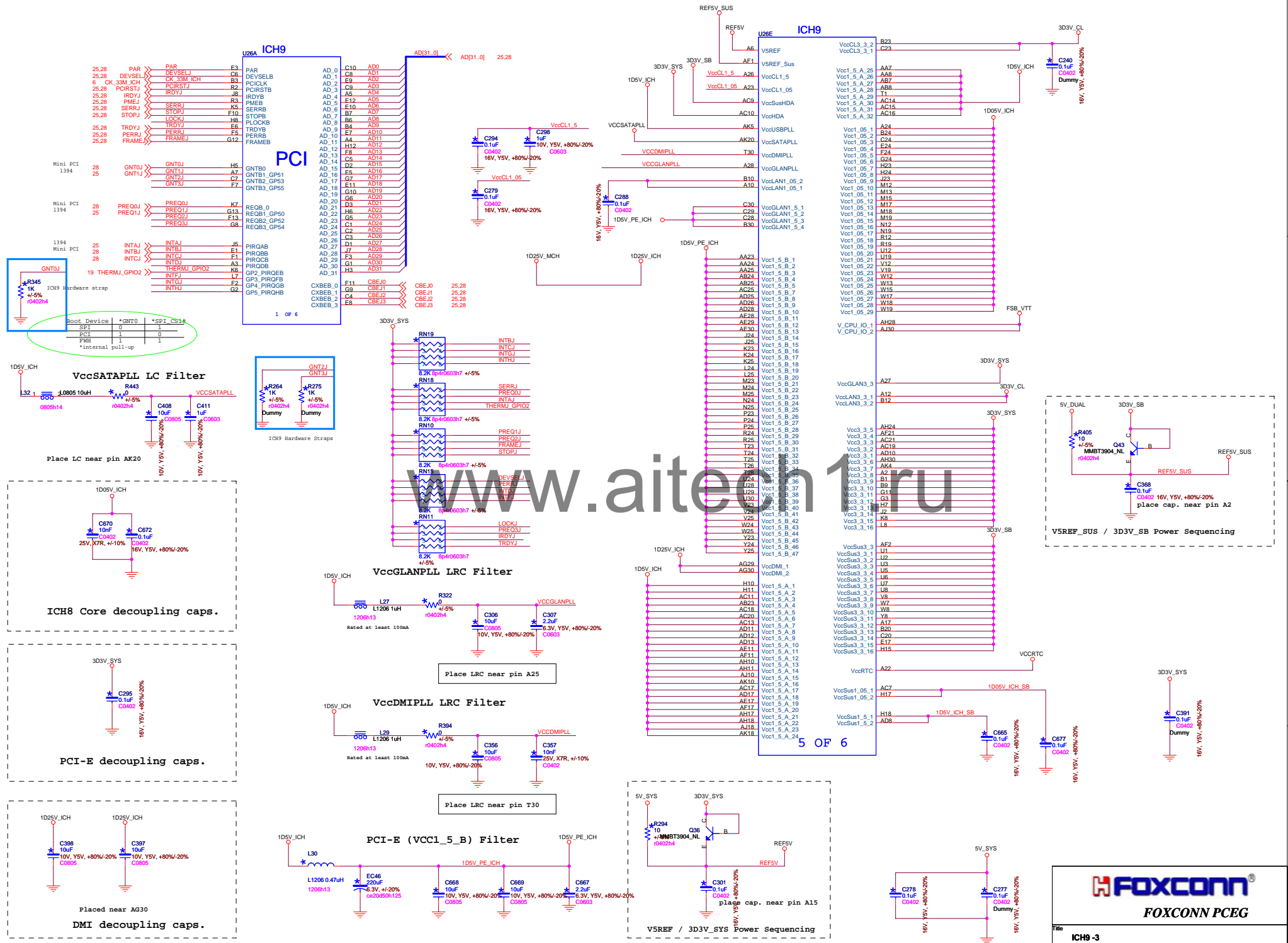
## HOTPLUG DETECTION

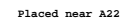
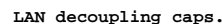
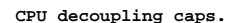
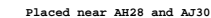
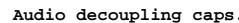
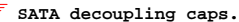


Title			
HDMI_DVI_VGA_CONN			
Size	Document Number		
C	G33S01		
Date:	Wednesday, July 04, 2007	Sheet	17 of 43







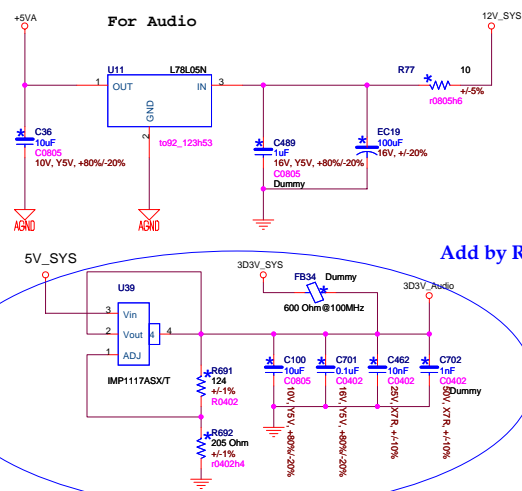
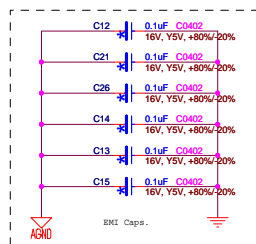


PCI decoupling caps.

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***ALC888***



Add by Roger 021007



Title			
HDA Codec ALC888-1			
Size	Document Number		
C	G33S01		
Date:	Tuesday, June 12, 2007	Sheet	22 of 43

## Digital Area

## Analog Area

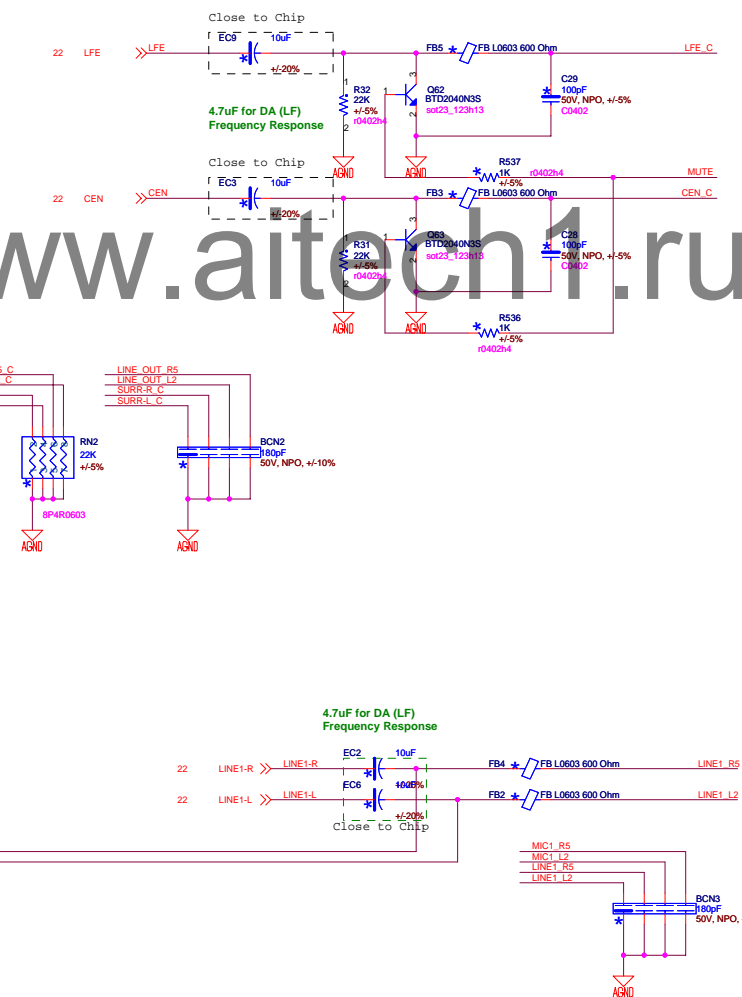
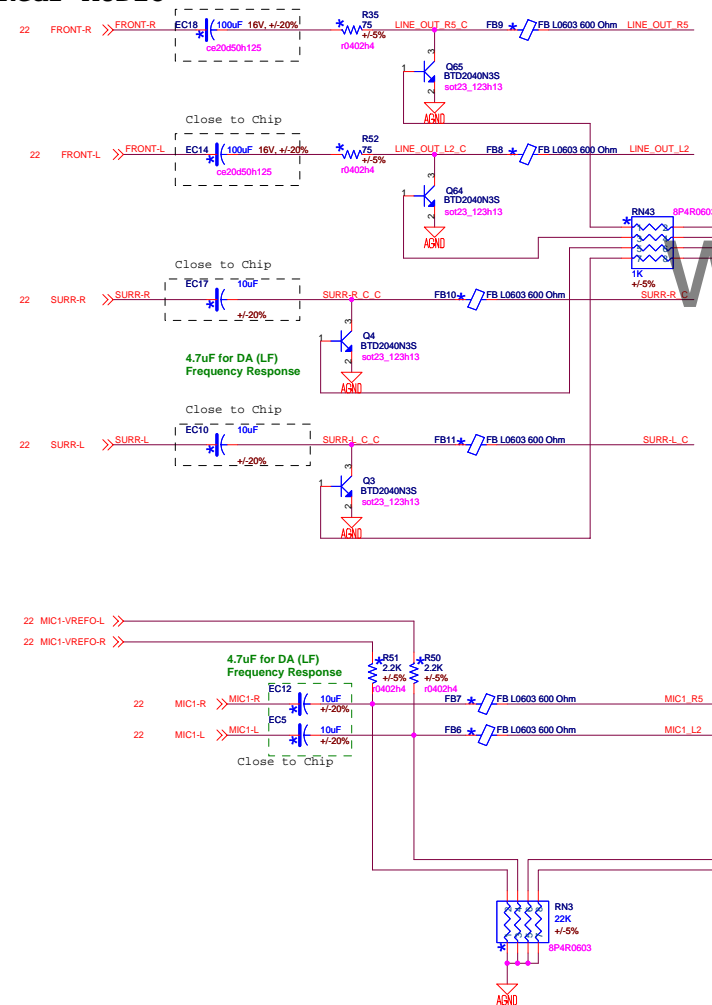
## FRONT AUDIO HEADER

Control by software driver and S/B GPIO.  
GPIO#0 driver low at:  
1).Initial state  
2).Suspend to S1  
3).Resume from S1.

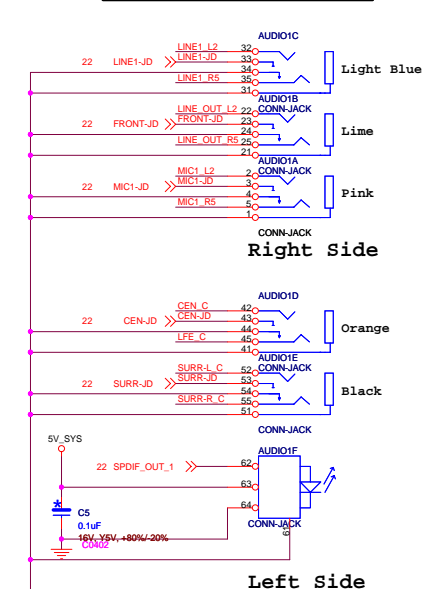
### Control line

### Control circuit

### Rear AUDIO



### 6 Azalia Audio Jacks



**FOXCONN**

**FOXCONN PCEG**

File: HDA Codec ALC888-2

Size: C

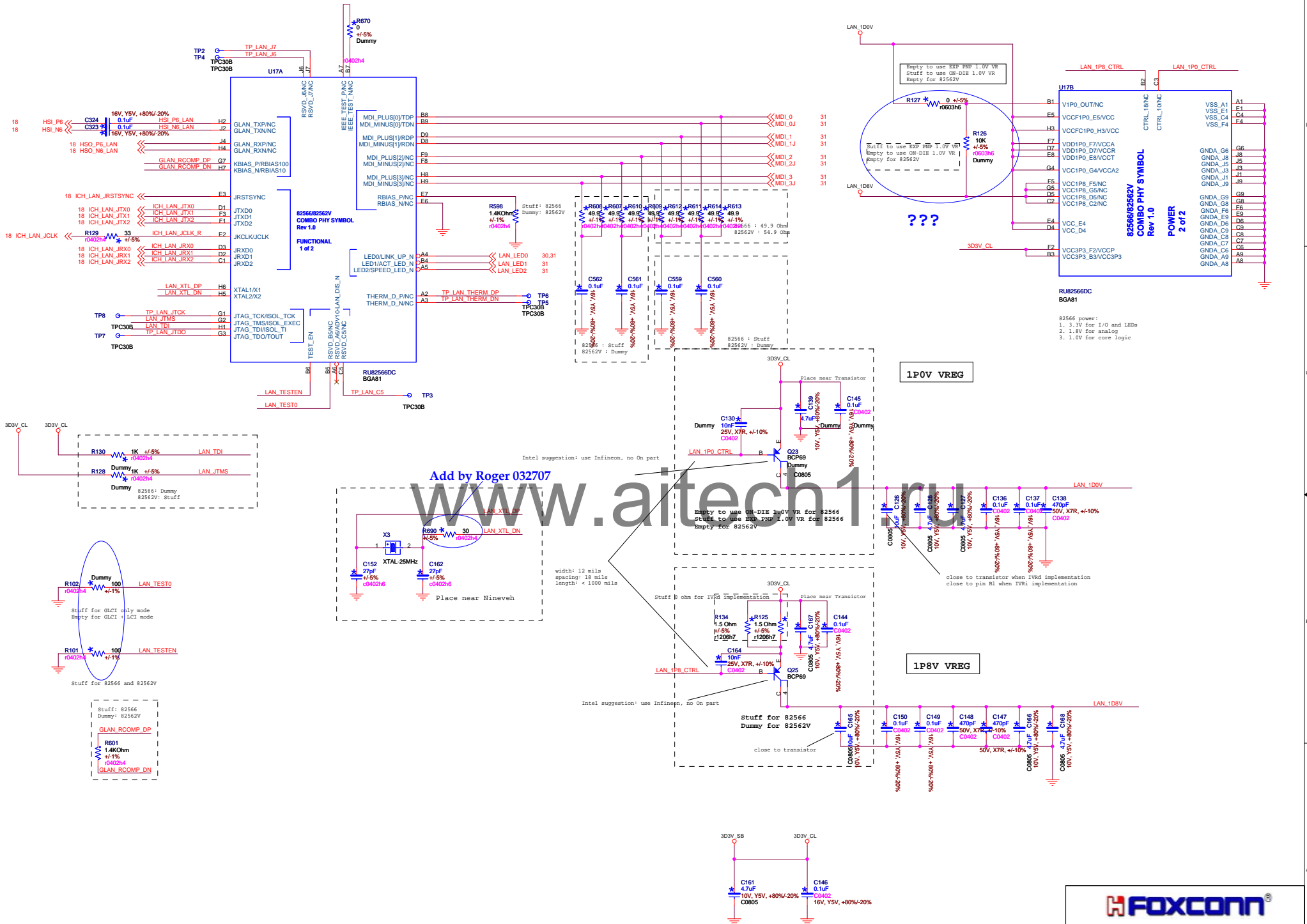
Document Number: **G33S01**

Date: Tuesday, June 12, 2007

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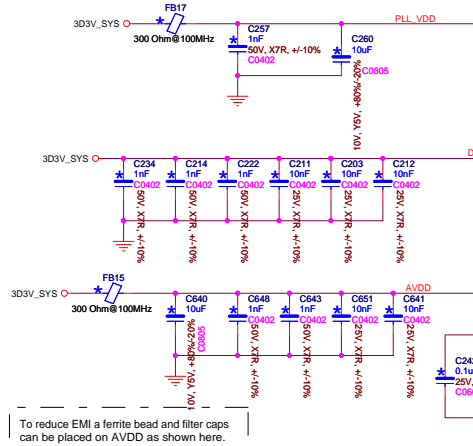
Rev: A



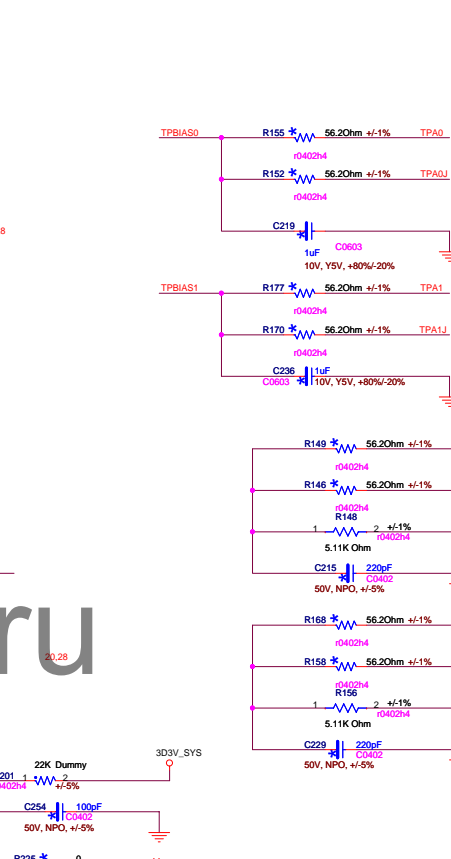
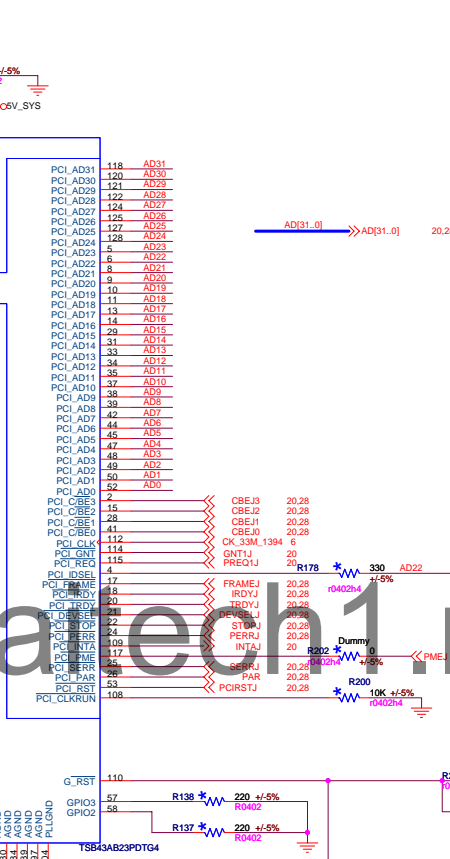
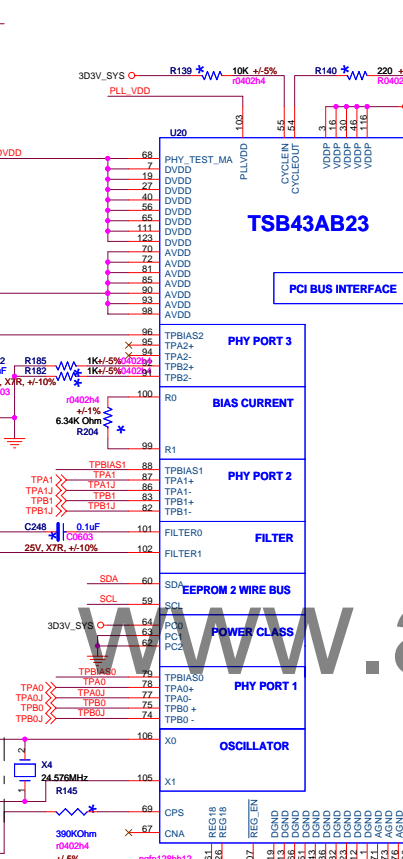
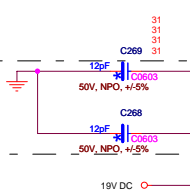




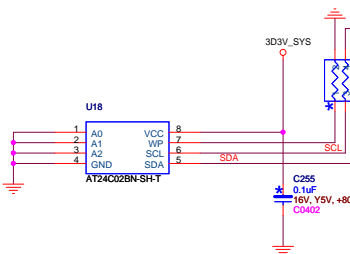
To reduce EMI and jitter a ferrite bead and filter caps can be placed on PLLVDD as shown here.

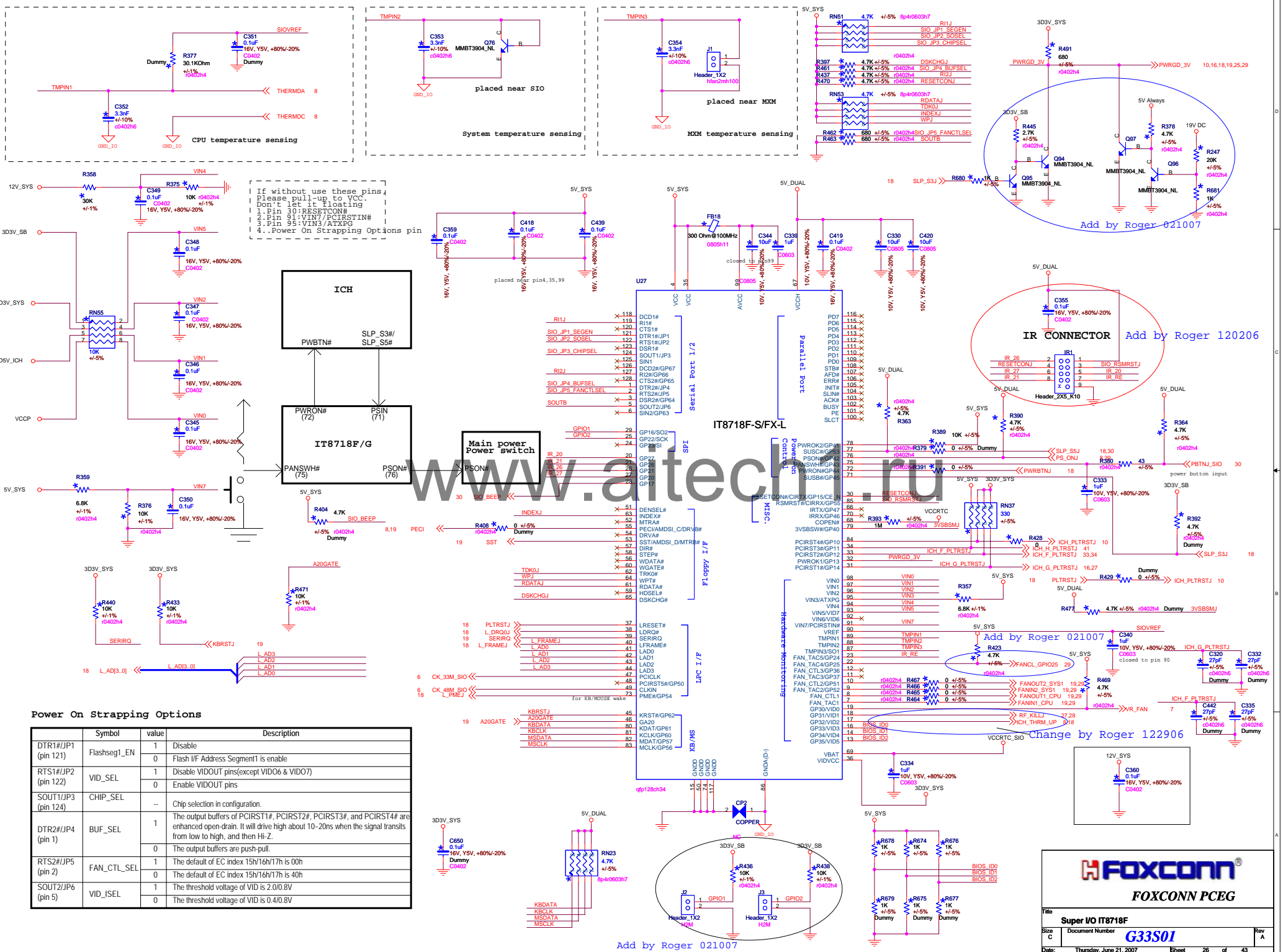


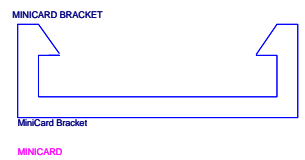
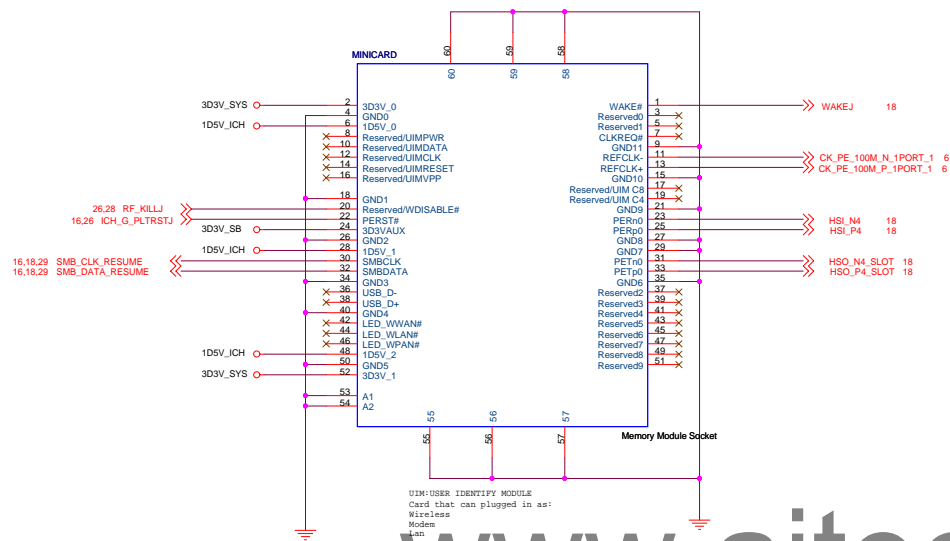
Crystal Requirements:  
 [ ] The crystal capacitive load (CL) should be between 10pF and 12pF  
 [ ] Crystal accuracy should be under 100PPM for process and temp combined  
 [ ] Parallel Resonance  
 [ ] Fundamental Mode  
 The value of the termination capacitors on each leg of the crystal to ground should be sized using the following formula: C Termination = (Crystal Load Capacitance - 4pF) X 2



GRST# signal should be asserted for a minimum of 2 ms after power is applied and stable to the TSB43AB23. The reset can be derived from POR or system logic. If supporting wake from D3aux this signal should not be asserted when resuming from D3.  
 Alternative reset options are provided as design options. The preferred reset option is to use a signal from system logic, if that is not possible then option 1 is preferred over option 2.

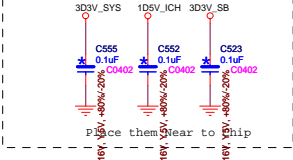
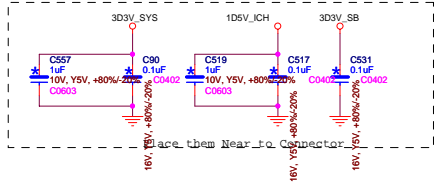


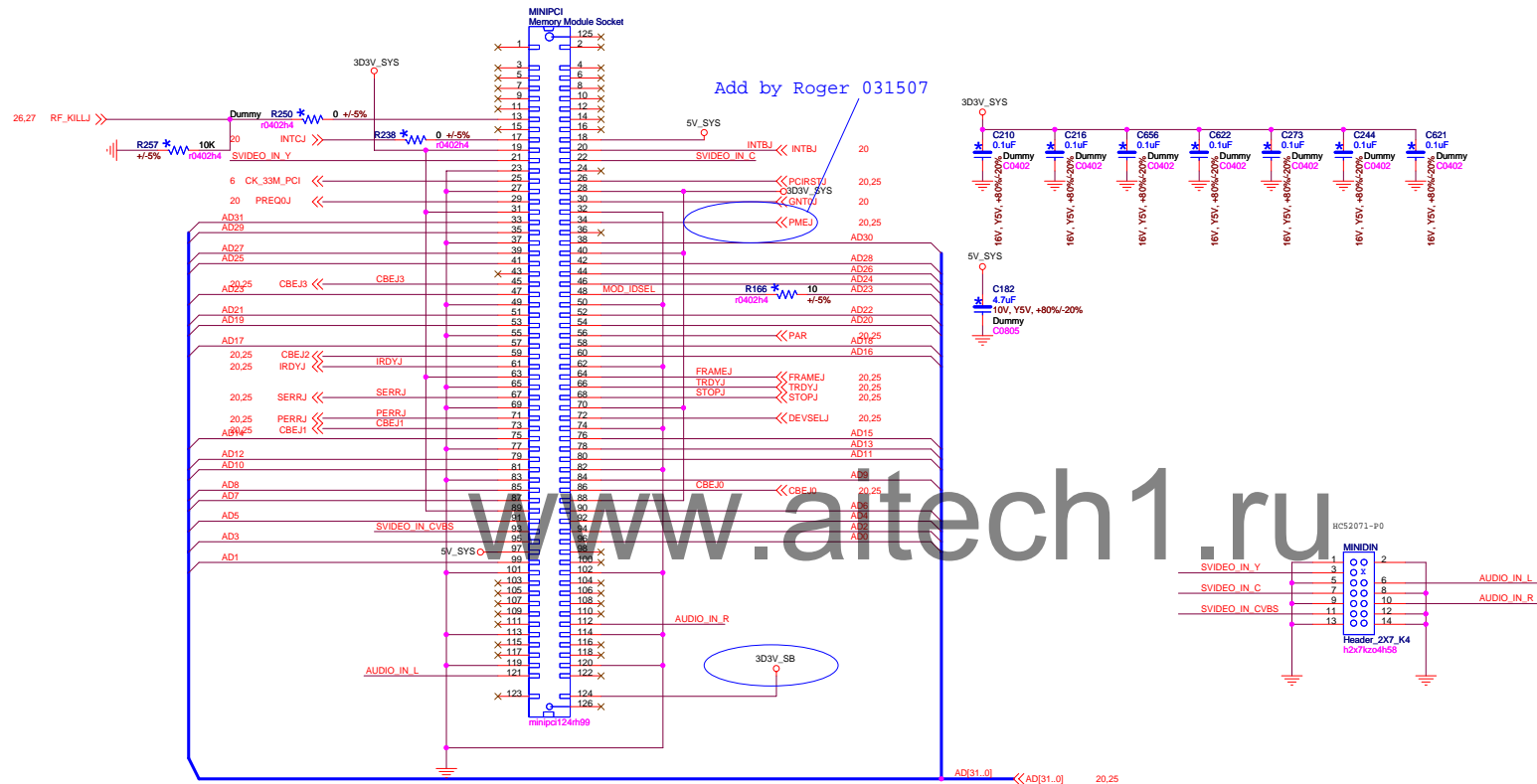




UIM-USER IDENTIFY MODULE  
Card that can plugged in as:  
Wireless  
Modem  
LAN

HOW TO IDENTIFY ITS POWER REQUIREMENT?  
Does it need 3.3V?  
I'm not sure 3.3V is used?





**SM Bus Bridge**

10,16,15,19,25,26 PWRGD\_3V

3D3V\_SB

12V\_SYS

3D3V\_SYS

SMB\_DATA\_RESUME

SMB\_CLK\_RESUME

SMB\_DATA\_MAIN

SMB\_CLK\_MAIN

6.14 SMB\_DATA\_MAIN

6.14 SMB\_CLK\_MAIN

16,18,27

16,18,27

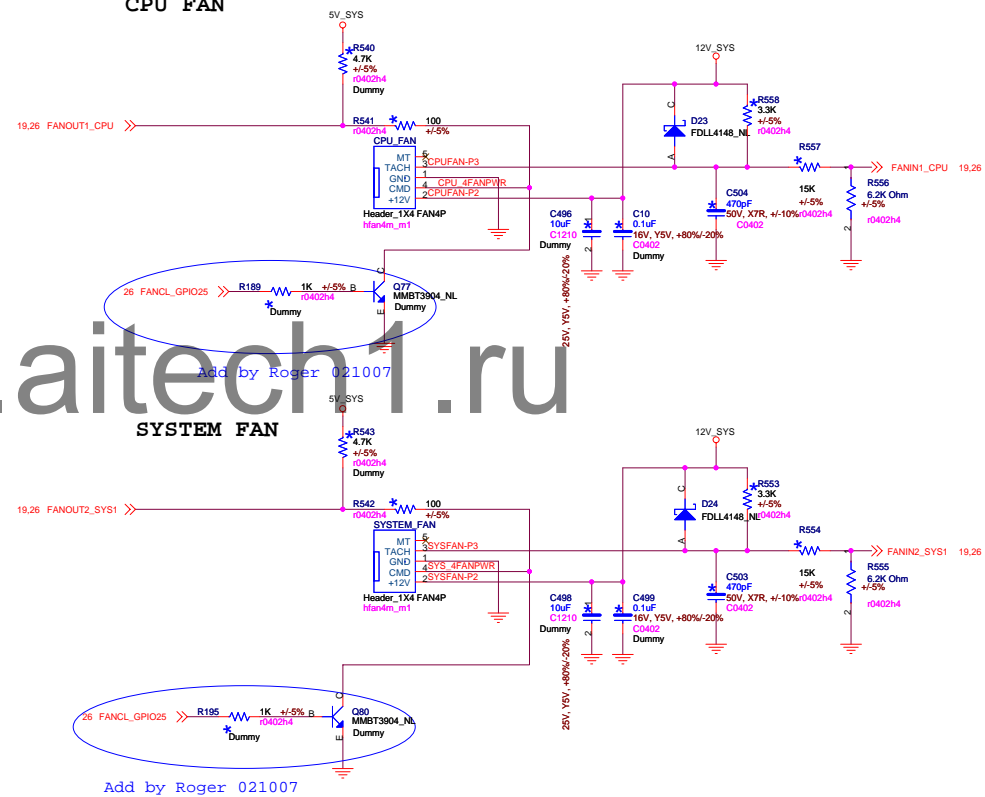
for Clock Generator/D106a

for PCI-E x16/ICH8/LAM/PCI/PCI-E x1/Over Clock

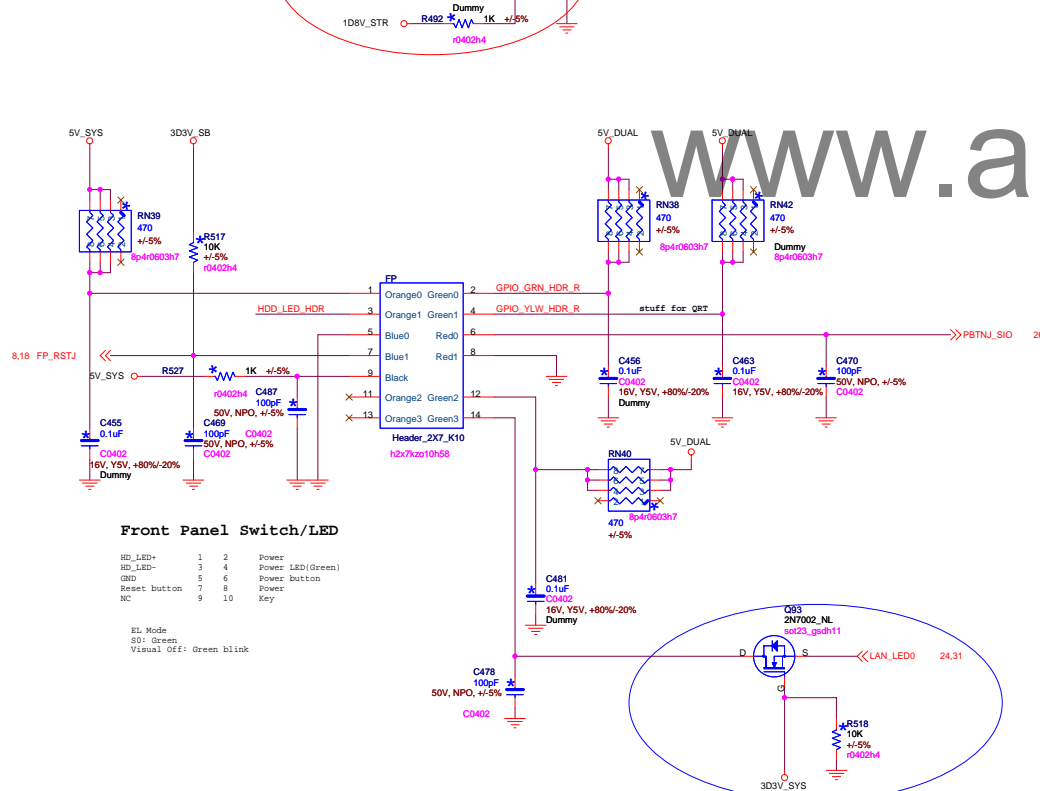
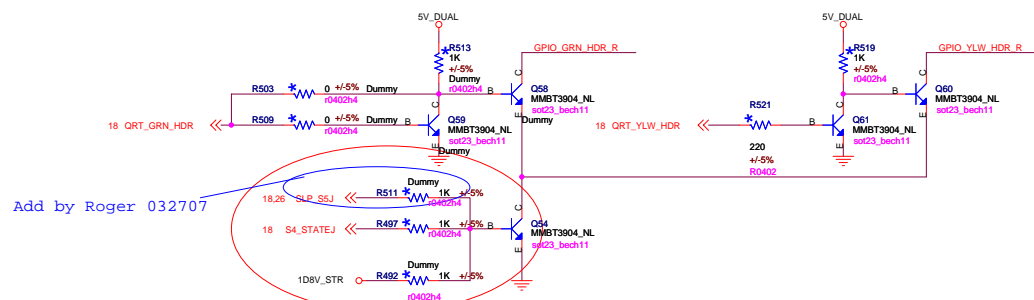
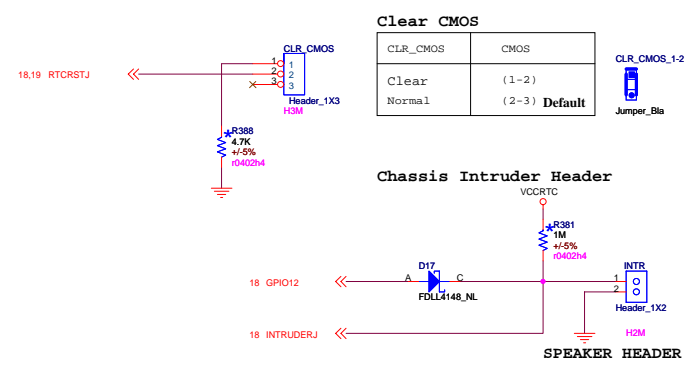
Add by Roger 03300

www

CPU FAN



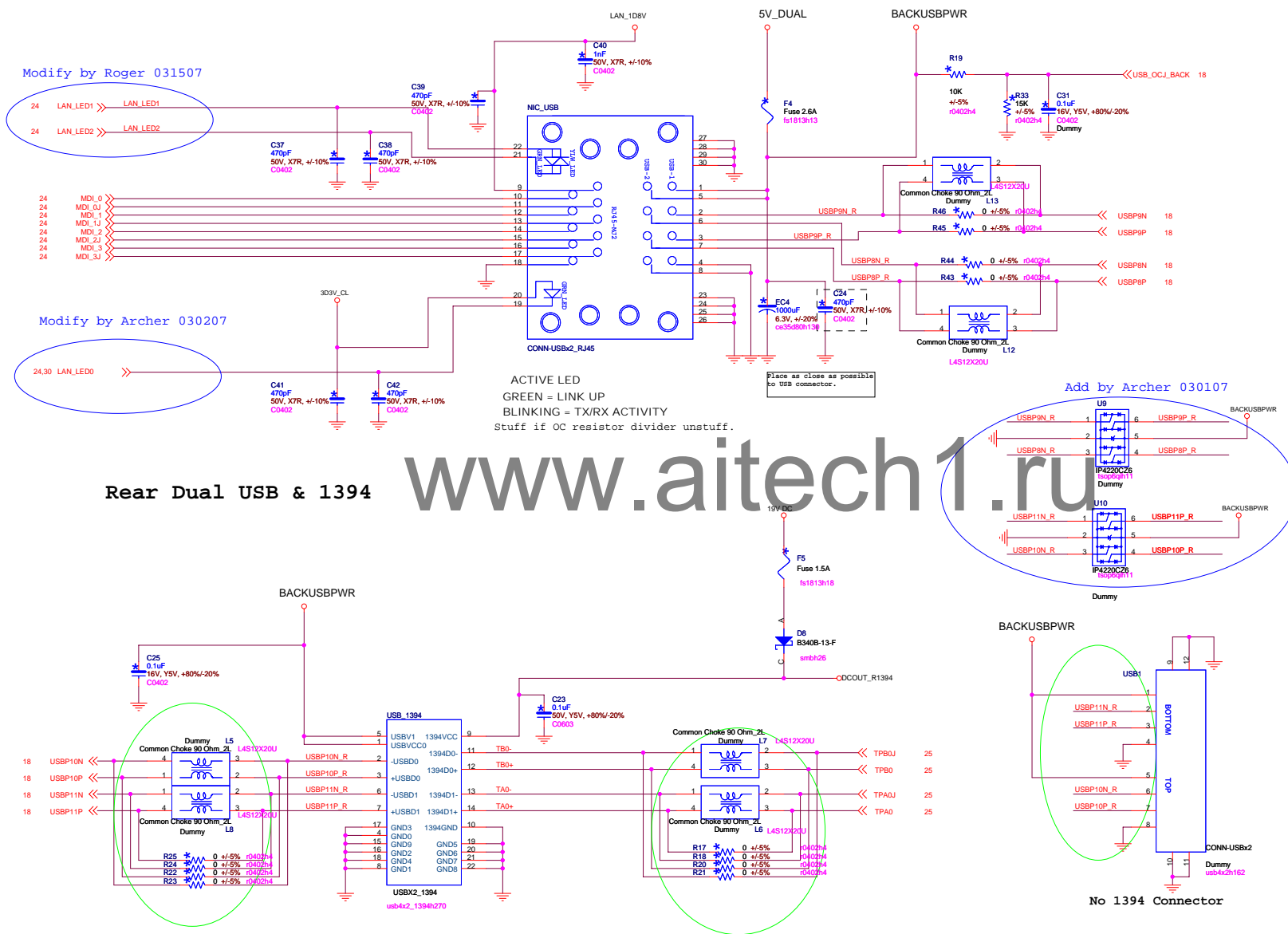
Add by Roger 021007

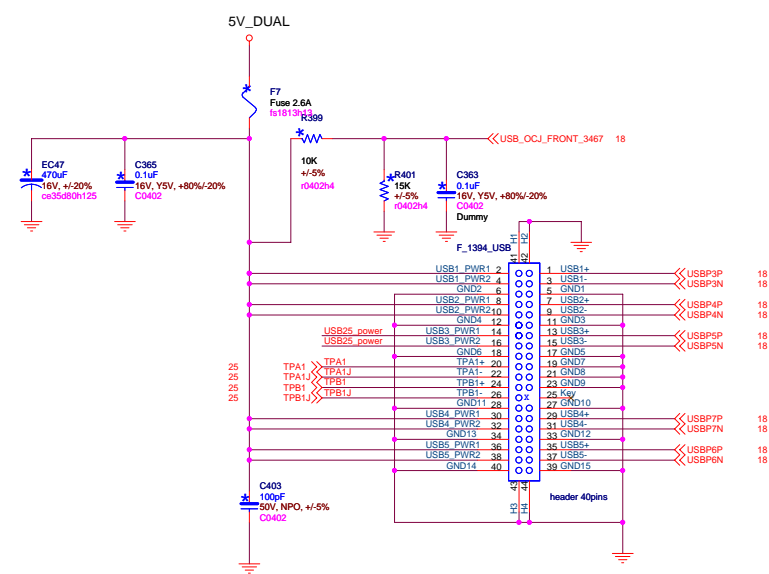
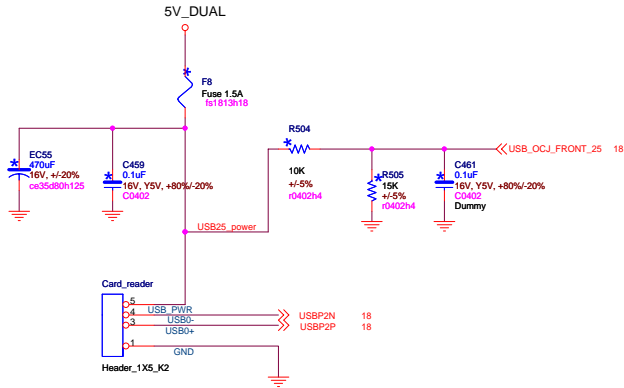


Modify by Archer 030207

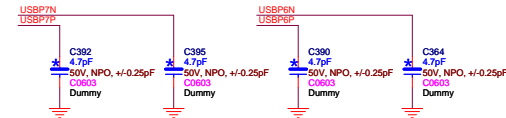
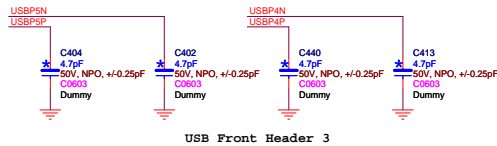
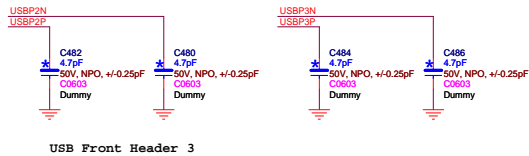
SPEED LED	
LINK 10M	OFF
LINK 100M	YELLOW
LINK 1000M	GREEN

# **BACK PANEL ( LAN + 2 USB Connector )** **USE CONNECTOR(Foxconn P/N: JFM38U1A-21U5-4N) WITH GIGABIT DESIGN**





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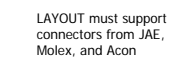


**LAYOUT RULES:**

- Route traces with 100 Ohm Differential Impedance
- Avoid placing GND Copper or traces adjacent to TMDS Trace
- Put these 4 resistors and 4 capacitors as close as possible to the TMDS output pins of the Sil1392

Route traces with 100 Ohm Differential Impedance  
Avoid placing GND Copper or traces adjacent to TMDS Trace  
Put these 4 resistors and 4 capacitors as close as possible  
to the TMDS output pins of the Si11392

R618 300Ω  $\pm 5\%$  C577 16V\_Y5V, +80%/20%  
 C577 10.1uF C0402  
 HDMI\_TXA2P\_1392 16,17  
 HDMI\_TXA2N\_1392 16,17  
 R617 300Ω  $\pm 5\%$  C575 16V\_Y5V, +80%/20%  
 C575 10.1uF C0402  
 HDMI\_TXAP1\_1392 16,17  
 R619 300Ω  $\pm 5\%$  C585 16V\_Y5V, +80%/20%  
 C585 10.1uF C0402  
 HDMI\_TXAN1\_1392 16,17  
 HDMI\_TXAPO\_1392 16,17  
 R616 300Ω  $\pm 5\%$  C574 16V\_Y5V, +80%/20%  
 C574 10.1uF C0402  
 HDMI\_TXAN0\_1392 16,17  
 HDMI\_TXCAP\_1392 16,17  
 R589 1K R615  $\pm 5\%$  750 AVCC  
 C589 0.047uF C0402  
 HDMI\_TXCN0\_1392 16,17  
 HDMI\_TXMDS\_HPD\_1392 16,17



**R602** 22  $\ll$  SPDIF\_OUT\_2\_C 16  
r0402n4 +5%  
Dummy

R605 33 \* +5% r0402n4  
R606 33 +5% r0402n4  $\gg$  CH\_AUD\_SDOUT 18,2  
R602 33 +5% r0402n4  $\gg$  CH\_AUD\_SYNC 18,22  
R600 22 +5% r0402n4  $\gg$  CH\_AUD\_SDIÑO 18  
R600 22 +5% r0402n4  $\gg$  CH\_AUD\_RSTJ 18,22

HD\_IOPWR voltage  
60 Ohm should be same as HD  
audio or SPDIF source

RX1

TX0-3

From GMCH

DVI Output

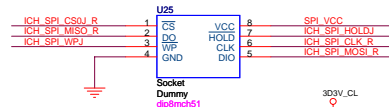
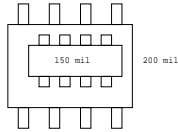
Remove by Roger 010207



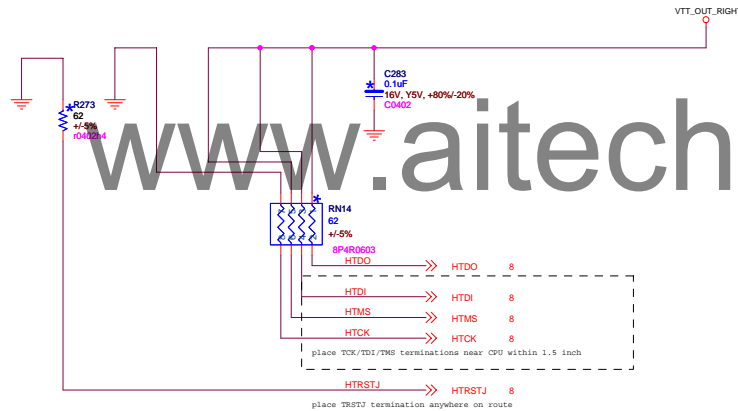
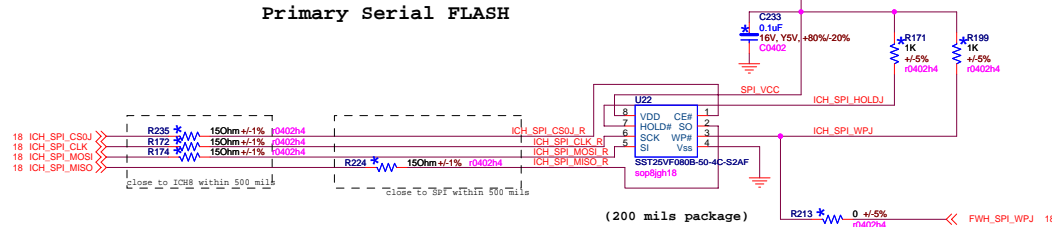
FOXCONN PCEG

Title			Reserved
Size	Document Number	G33S01	
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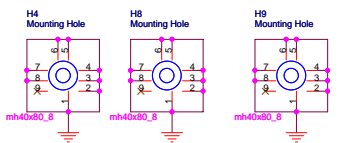
SO8 MN and MW co-layout



## Primary Serial FLASH

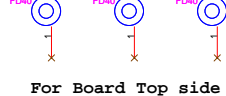


H16  
FMARK  
mh40x80



For Daughter board

H3  
FMARK  
FD40



For Board Top side

H2  
FMARK  
FD40



H7  
FMARK  
FD40



H10  
FMARK  
FD40



H15  
FMARK  
FD40



For Board Bottom side

H5  
FMARK  
FD40



H6  
FMARK  
FD40



For CPU

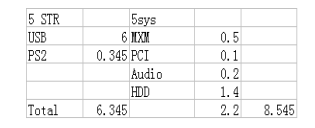
H13  
FMARK  
FD40

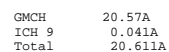


**FOXCONN**

FOXCONN PCEG

Serial FLASH		
Size	Document Number	Rev
C	G33S01	A
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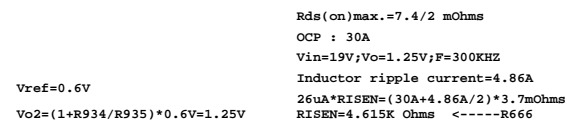




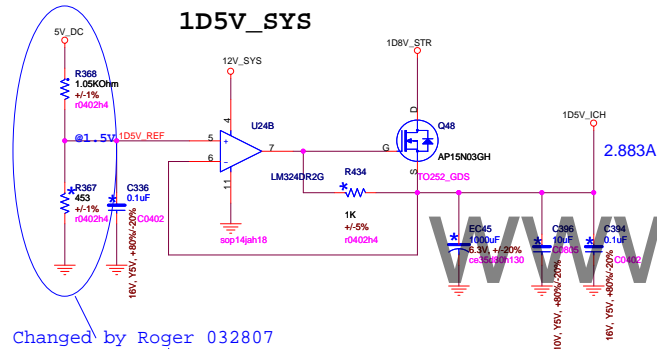
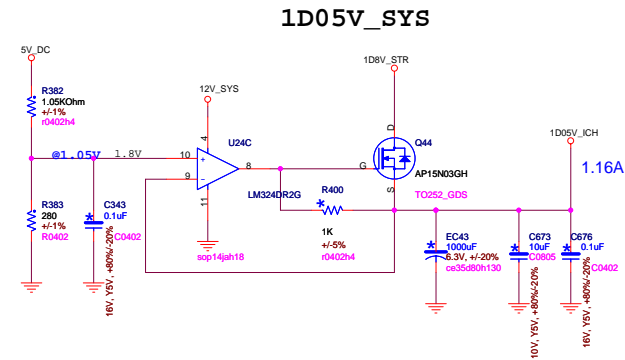
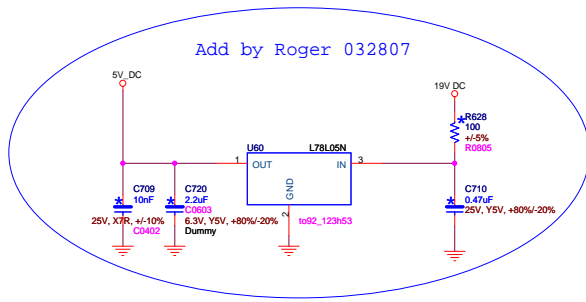
1.8 STR	
DDR	4.7
DDR(0.9V)	0.6
GMCH	4.18
MXM	3.5
1.8 to FSB(linear)	5.8
1.8 to 1.5(linear)	2.883
1.8 to 1.05(linear)	1.16
Total	22.823

Set 3.3k



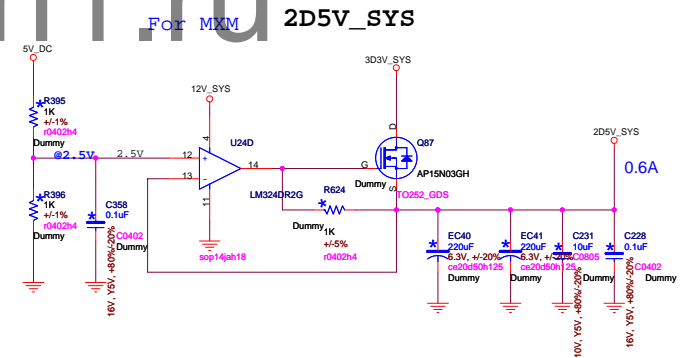
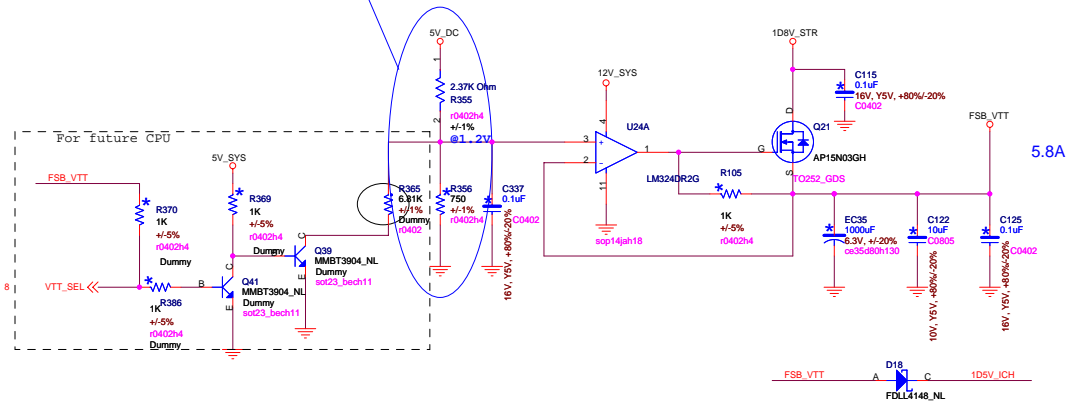






Changed by Roger 032807

### FSB\_VTT



**FOXCONN**

FOXCONN PCEG

File		
1D5V/1D05V/FSB/MXM2D5V		
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# ICH9 GPIO Summary

Name	Power Well	Type	Default	Use Description
GPIO0	3.3V	I/O	Define	FP_AUD_DETECT
GPIO1	3.3V	I/O	Define	FANIN2_SYS1 TACH1
GPIO2	5V	I/OD	Low	PIRQE#, No use pull high
GPIO3	5V	I/OD	Low	PIRQF#, No use pull high
GPIO4	5V	I/OD	Low	PIRQG#, No use pull high
GPIO5	5V	I/OD	Low	PIRQH#, No use pull high
GPIO6	3.3V	I/O	Define	TACH_2, No use pull high
GPIO7	3.3V	I/O	Define	TACH_3, No use pull high
GPIO8	3.3V_SB	I/O	Define	OBR
GPIO9	3.3V_SB	I/O	Define	WOL_ONLY
GPIO10	3.3V_SB	I/O	Define	Unused(pull-up)
GPIO11	3.3V_SB	I/O	Low	SMBALERT#, pull high
GPIO12	3.3V_SB	I/O	Low	INTRUDERJ
GPIO13	3.3V_SB	I/O	Low	L_PME#
GPIO14	3.3V_SB	I/O	Define	Unused(pull-up)
GPIO15	3.3V_SB	I/O	High	CK_PCI_STOP
GPIO16	3.3V	I/O	Low	Unused(NC)
GPIO17	3.3V	I/O	Define	FANIN1_CPU TACH0
GPIO18	3.3V	I/O	High	Unused(NC)
GPIO19	3.3V	I/O	Define	SATA_1GP, No use pull high
GPIO20	3.3V	I/O	High	Unused(NC)
GPIO21	3.3V	I/O	Define	SATA_0GP
GPIO22	3.3V	I/O	Define	Unused(pull-up)
GPIO23	3.3V	I/O	Define	LDRQ1#, NC
GPIO24	3.3V_SB	I/O	High-Z	No use pull high
GPIO25	3.3V_SB	I/O	High	CK_CPU_STOP
GPIO26	3.3V_SB	I/O	Low	S4_STATE#
GPIO27	3.3V_SB	I/O	Low	QRT_STATE0
GPIO28	3.3V_SB	I/O	Low	QRT_STATE1
GPIO29	3.3V_SB	I/O	Low	USB_OC5_FRONT#
GPIO30	3.3V_SB	I/O	Low	USB_OC6_FRONT#
GPIO31	3.3V_SB	I/O	Low	USB_OC7_FRONT#
GPIO32	3.3V	I/O	High	Unused(NC)
GPIO33	3.3V	I/O	High	Controller
GPIO34	3.3V	I/O	Low	Unused(NC)
GPIO35	3.3V	I/O	Low	Unused(NC)
GPIO36	3.3V	I/O	Define	SATA_2GP
GPIO37	3.3V	I/O	Define	SATA_3GP, No use NC
GPIO38	3.3V	I/O	Define	Unused(pull-up)
GPIO39	3.3V	I/O	Define	Unused(pull-down)
GPIO40	3.3V_SB	I/O	Define	USB_OC1_FRONT#
GPIO41	3.3V_SB	I/O	Define	USB_OC2_FRONT#
GPIO42	3.3V_SB	I/O	Define	USB_OC3_FRONT#
GPIO43	3.3V_SB	I/O	Define	USB_OC4_FRONT#
GPIO44	3.3V_SB	N/A	Define	USB_OC8_BACK#
GPIO45	3.3V_SB	N/A	Define	USB_OC9_BACK#
GPIO46	3.3V_SB	N/A	Define	USB_OC10_BACK_LAN#
GPIO47	3.3V_SB	N/A	Define	USB_OC11_BACK_LAN#
GPIO48	3.3V	I/O	Define	Unused(pull-up)
GPIO49	3.3V	I/O	Define	DMI_STRAP(pull-down)
GPIO50	5.5V	I/O	Define	REQ_1#
GPIO51	3.3V	I/O	High-Z	GNT1J
GPIO52	5.5V	I/O	Define	REQ_2#,No use pull high
GPIO53	3.3V	I/O	High-Z	GNT1J,No use
GPIO54	5.5V	I/O	Define	REQ_3#, No use pull high
GPIO55	3.3V	I/O	High-Z	GNT2J,No use
GPIO56	3.3V_SB	I/O	High-Z	Unused(pull-up)
GPIO57	3.3V_SB	I/O	High-Z	FWH_SPI_WPJ
GPIO58	3.3V_SB	I/O	High-Z	Unused(pull-up)
GPIO59	3.3V_SB	I/O	Define	USB_OC0_FRONT#
GPIO60	3.3V_SB	I/O	High-Z	Unused(pull-up)

8/21 Initial schematics according to USA CB# v0.7  
8/22 Add AMT\_LMD function in Reserved page  
8/23 Change ALC 883 to 888 in HDA Codec page  
8/25 Change ICH\_SYNC, ICH\_SDIN2, ICH\_SDOUT, ICH\_SDOUT\_R,  
ICH\_SYNC\_R net name to ICH\_AUD\_SYNC, ICH\_AUD\_SDIN2,  
ICH\_AUD\_SDOUT, ICH\_AUD\_SDOUT\_R, ICH\_AUD\_SYNC\_R  
in ICH9-1 and HDA Codec page

Del VID0 to VID 7 in IT8718 page

Add VID\_SELECT(AN7) connect to 0 ohm to VRD6321 in  
UGA775-1 and VRD 6312 page

8/30 Change the MLCC cap connected to ths audio jack  
to EC in HDA Codec page for Vista

8/31 Change routing

Add the fourth phase in VRD 6312 page

9/2 Add S4\_STATE circuit in reserved-2 page

Modify 5V\_DUAL circuit in page 17

Modify the USB power circuit from 5V\_DUAL to USB\_DUAL

9/5 Modify IT8718 separating the analog GND and digital GND

Del net CK\_CPU\_STOP and CK\_FCI\_STOP in CK505 page

9/6 Add 1000uF to 5V\_SB\_SYS in page 30

12/28 Modify SCH from BLN01 to G33S01 FAB A SCH

2/10/07 Modify SCH from FAB A to G33S01 FAB B SCH

3/26/07 Modify SCH from FAB B to G33S01 FAB C SCH

1.04/03/2007(1)Remove R268, R8165 and Q29; (2)Add R360 and R361; (3)Reserve R360 and R361.

For Intel recommendation.

2.04/03/2007(1)Delete R305;(2)Connect R\_TESTTH1\_A to TESTTH1\_12.

For Intel recommendation.

3.04/03/2007 (1)Add Q98 and Q100;(2)Reserve Q98 and Q100.

For MDM HDMI DDC 3.3V to 5V level shift.

4.04/03/2007 (1)Add R704;(2)Remove R704.

For MDM FRBMT.

5.04/04/2007(1)Not connect USB-pin5 to 5V\_SYS;(2)Not connect USB-pin4 to DVI\_TMDS\_HPD\_1362;(3)Connect USB-pin4 to 5V\_HDMI.

For Fixing onboard HDMI SI issue.

6.04/04/2007(1)Add D25 and R682;(2)Reserve D25 for MDM sku.

For meeting NOT\_PLUG\_DETECT\_HDMI SPEC.

7.04/04/2007(1)Add D26, R38, R689 and C102;(2)Reserve D26 for MDM;(3)Remove R38 and C102.

For meeting NOT\_PLUG\_DETECT\_DVI SPEC.

8.04/04/2007(1)Connect MDM VGA IDC to Q85 and Q86;

For MDM VGA DDC 3.3V to 5V level shift.

9.04/05/2007(1)Add D27 D28 and R430;(2)Remove D27 D28 and R430 .

For adding THERMAL\_MDM function.

10.04/05/2007(1)Connect PME1 to MINIPCI;(2) Connect 3D3V\_SB to MINIPCI;

For adding MINIPCI PME function.

11.04/05/2007(1)Add R511 and use SLP\_S52 to control power LED;(2) Remove R511.

For Fixing power LED issue.

12.04/05/2007(1)Connect LAN\_LED0 to NIC\_USB directly;(2)Connect LAN\_LED1 from NIC\_USB pin21 to pin 22;(3)Connect LAN\_LED2 from NIC\_USB pin22 to pin 21.

For following Acer PSB.

13.04/05/2007(1)Add U40, R699, R700, C703, C704, C707, and C708;(2)Reserve U40, R699, R700, C703, C704, C707, and C708 for onboard HDMI and DVI sku;(3)Remove Q84.

For improving 1D05V\_SYS qualification and fixing DVI SI issue.

14.04/05/2007(1)Change SI11362A and SI11392 3.3V power from 3D3V\_SYS to 3D3V\_Audio;(2)Add C718 and C719;(3)Reserve C718 and C719;

(4)Change R635, R636, R637 and R646 from 300ohm to 120ohm;(5)Change R623 from 360ohm to 240ohm.

For Fixing DVI SI issue.

16.04/05/2007(1)Add U60, R628, C709, R710 and C720;(2)Reserve U60, R628, C709, R710;(3)Remove C720;(4)Use 5V\_DC as 1D05V\_ICH, PSB\_VTT, 1D05V\_ICH and 2D5V\_SYS reference voltage.

For improving 1D05V\_ICH, PSB\_VTT, 1D05V\_ICH and 2D5V\_SYS qualification.

17.04/05/2007(1)Add U59, Q31, Q102, Q103, Q104, R595, R696, R697, R698, R705, R706, R707, R708, R709, R710 and R97;(2)Reserve U59, Q31, Q102, R595, R696, R697, R707, R708;

(3)Remove Q103, Q104, R698, R705, R706, R709, R710 and R97.

For 1D05V high and low voltage protect.

18.04/05/2007(1)Reserve R398, R402, Q53 and Q99;

For adding CPU temperature warning function.

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